Dan

32-5004-B

INSTRUCTION MANUAL

MODEL 3400

4-½ DIGIT PROGRAMMABLE MULTIMETER

DATA PRECISION

...years ahead

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INSTRUCTION MANUAL

MODEL 3400

4-½ DIGIT PROGRAMMABLE MULTIMETER

Principles of Operation

Specifications

Maintenance Data

Schematics

Parts Lists

DATA PRECISION
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Frontispiece -- Model 3400 Programmable Digital Multimeter

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INTRODUCTION & SPECIFICATIONS

1.1 GENERAL DESCRIPTION

Data Precision Model 3400DMM is a local-or remote-programmable 4-1/2 digit digital multimeter, providing up to 12 conversion measurements per second with high accuracy performance. It incorporates Data Precision's Tri-Phasic™ A/D Conversion, Isopolar™ referencing, and 2- or 4-wire Ratiohmic resistance measurements, as well as auto-zero circuitry that compensates for instrument drift before each and every conversion. Each Model 3400DMM includes all interface signals for remote programming of range (selected range or auto-range) and mode of signal measurement (DCV, ACV, kΩ, or Voltage Ratio), for external trigger control or holding function, and for BCD-formatted output data. All output data signals, as well as conversion status (for remote recording or display) are available as DTL/TTL compatible voltage levels. Complete measurement and control instrumentation is provided as part of the standard Model 3400DMM equipment.

Complete, detailed performance specifications are reproduced in paragraph 1.3 of this chapter.

1.2 BRIEF OPERATING DESCRIPTION

1.2.1 Tri-Phasic A/D Conversion

a. Conversion of an analog signal into a digital form is accomplished in a combination of analog and digital circuitry. The analog portion of the Tri-Phasic A/D conversion is illustrated in Figure 1-1. Programming of the A/D is accomplished by digital logic driven by a master clock and by signals derived from the analog circuit operation.

b. Tri-Phasic A/D conversion processes the analog signal into a proportionate time interval in the circuit of Figure 1-1 in the following 3 steps (or phases):

Phase 1: The analog circuitry is "zeroed" to obtain an off-zero compensation value.

Phase 2: The unknown analog signal, corrected for the compensation determined in phase 1, is connected so that the net value charges an integrator capacitor for a fixed number of the time-base generator counts.

Phase 3: A precise voltage, of opposite polarity to the input signal, is connected to the circuit so that the charge on the integrator capacitor is reduced to zero. The time for this discharge phase is proportional to the value of the unknown analog input and controls the transfer of the digital count from the time base generator to the output register, and subsequent display.

c. During Phase 1 switch A is open (removing the analog input), switch B is closed (shorting A/D circuit input), switch C is closed (closing the loop around A2 and A3), and switches D,E, & F are open (removing the reference from the circuit and inhibiting "fast charge" of C_I).

The servo loop around A2 and A3 charges memory capacitor C_M to balance any non-zero signals generated in the circuit elements.

Phase 1 ends after some fixed time base interval, at which time the digital logic programmer changes the levels of control signals P1 and P2 so that the switches controlled by these levels change their states.

d. During Phase 2 switch A is closed (connecting the analog input to the A/D circuit), switches B & C are open (leaving C_M charged with the compensation for internal non-zero signals). Switches D, E, &F remain open.

Phase 2 ends after a fixed time base count, when the digital logic programmer changes the levels of P2 and P3, and switches controlled by these levels change their states.

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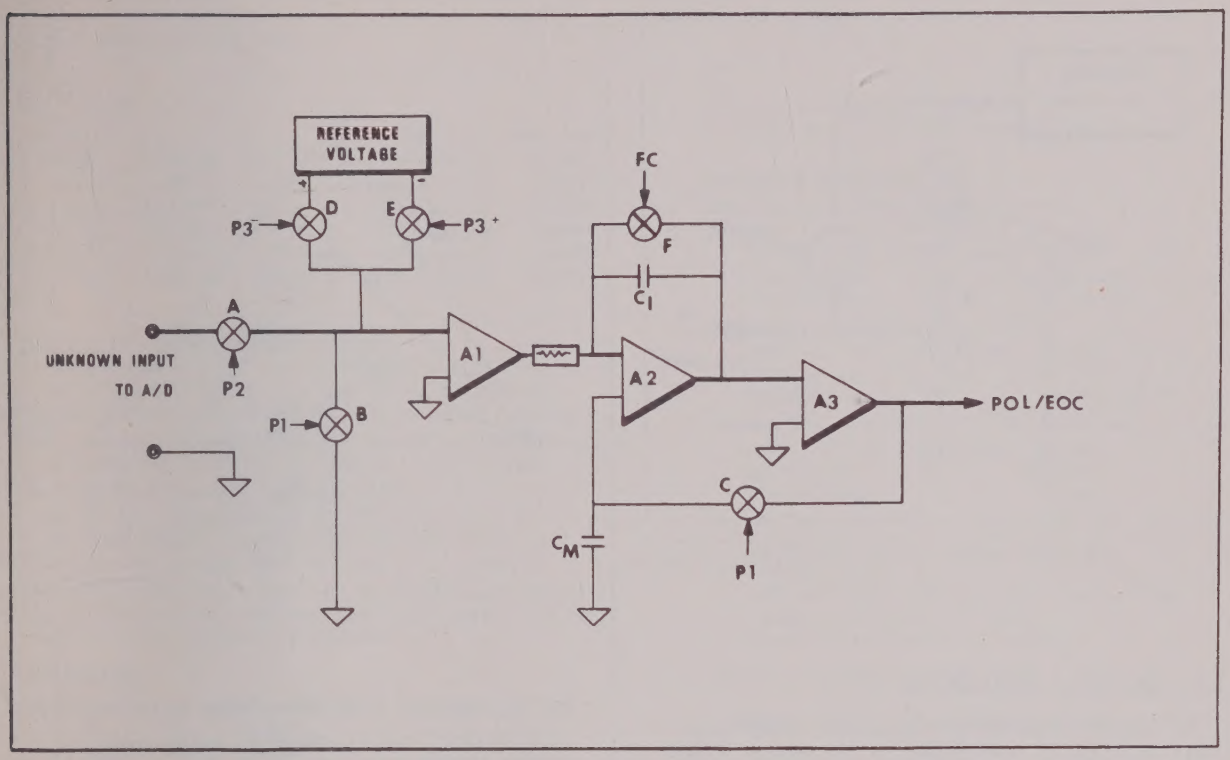

Fig. 1-1. Tri-Phasic A/D Converting simplified block diagram

e. During Phase 3 switch D is closed if the analog input is a negative input by the action of $P3^-$ (connecting a positive reference signal to the A/D input). If the analog input was a positive signal, then switch E would have been closed by signal $P3^+$. Thus, either $P3^-$ or $P3^+$ is active. The appropriate P3 signal is generated by the digital logic as a result of sensing the state of A3, whose output is identified in the illustration by POL/EOC, and this occurs at the end of Phase 2, when the analog input has been used to charge the integrator capacitor, C_I.

The duration of Phase 3 is determined by the change in state of A3, and indicated by the change in polarity of POL/EOC. The digital logic responds to this changing signal by initiating the Phase 1 actions.

1.2.2 Iso-Polar Referencing (Figure 1-2)

The conversion circuit described above utilizes either a positive or negative reference signal in its Phase 3 operation, as required by the polarity of the analog input. In the Data Precision circuitry, this reference is derived from a voltage of one magnitude, thus eliminating the need for separate independent calibration for positive and negative inputs (the "balance" problem encountered when the different polarities are derived independently).

Figure 1-2 illustrates the technique of isopolar referencing. The reference voltage, adjusted for the scaling required, charges a reference "battery" in the form of capacitor C_R.

When a positive reference is required, the negative capacitor terminal is connected to reference supply, placing the positive level on the line as input to the A/D.

When a negative reference is required, the positive capacitor terminal is grounded, and the negative terminal then places a negative voltage level on the A/D input line. The magnitude of the positive or negative value to the A/D is EXACTLY the voltage on the capacitor and does not vary with the polarity, hence the term, ISO-POLAR.

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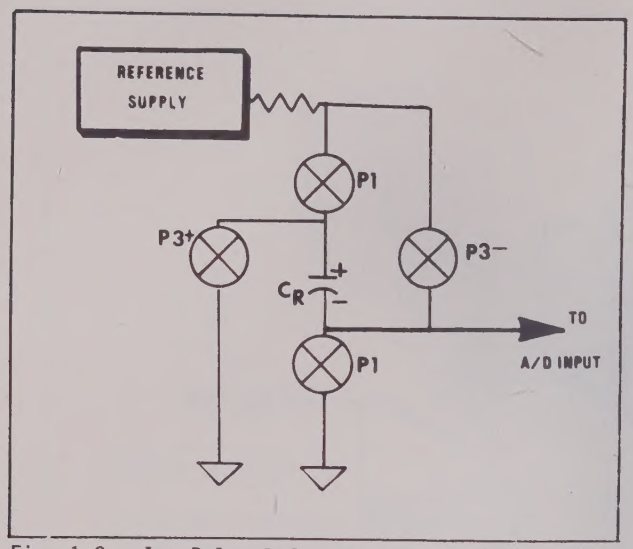


Fig. 1-2. Iso-Polar Referencing, simplified diagram

1.2.3 Ratiohmic Referencing

The Tri-Phasic A/D conversion technique is used to measure resistance in the manner illustrated by the simplified circuit of Figure 1-3. During Phase 2, the voltage input to the A/D is derived from the current flow through the unknown resistor. During Phase 3, the voltage input is derived from the effects of the SAME current through a precision resistor of known value. In other words, the integrating current during Phase 2 is proportional to the unknown resistance, while the integrating current during Phase 3 is determined by the value of the known precision resistor.

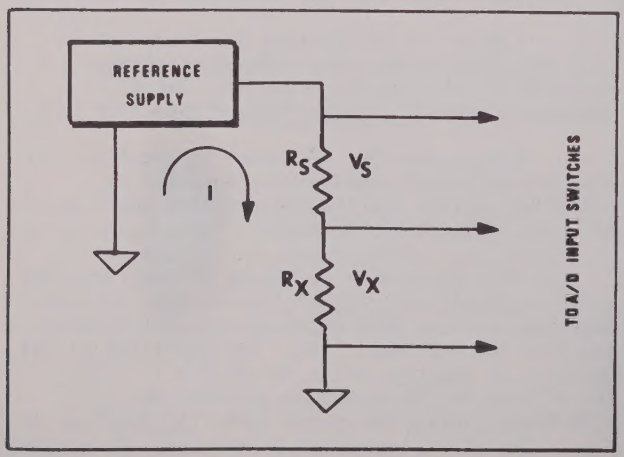
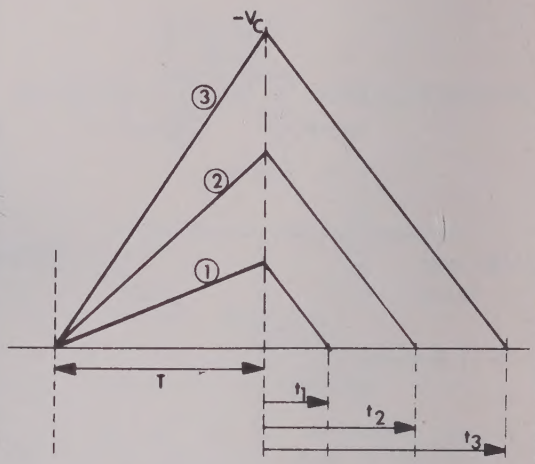


Fig. 1-3. Ratiohmic Referencing, simplified diagram



During Phase 2, peak of voltage V_C developed at end of Phase 2, is proportional to input R_X.

During Phase 3, time of ramp down is proportional to peak voltage reached at end of Phase 2.

$V_C = k_1 R_X \cdot I \cdot T$; $V_C = k_2 R_S \cdot I \cdot t$

$k_1 R_X I T = k_2 R_S I t$

$t = (R_X/R_S)K$

Fig. 1-4. Dual Slope System Timing Diagrams for Ratiohmic Mode

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1.3 SPECIFICATIONS

DC VOLTS

Nominal Range	Overrange	Resolution	Input Impedance	Max. Input Voltage
10000	±.19999	10 μV	>1,000 megohms	±1000V
1.0000	±1.9999	100 μV	>1,000 megohms	±1000V
10.000	±19.999	1mV	10 megohms	±1000V
100.00	±199.99	10mV	10 megohms	±1000V
1000.0	±1000.0	100mV	10 megohms	±1000V

Accuracy (all ranges, including overrange):
24 hours, 23°C ±5°C ±0.004% of rdg. ±1 l.s.d.
6 months, 23°C ±5°C ±0.007% of rdg. ±1 l.s.d.

Voltage Coefficient: ±0.00001% rdg./Volt (on 1000V range only).

Temperature Coefficient (0°C to 18°C and 28°C to 50°C, all ranges): (±0.001% rdg. ±0.0005% f.s.)/°C

Common Mode Rejection Ratios (minimum):
at DC, 160 dB with unbalanced 1000 Ohm source.
at 60 Hz, 120 dB with unbalanced 1000 Ohm source.

Common-Mode Voltage: 500V DC (or peak AC) maximum.

Normal-Mode Rejection: 60 dB at 60 Hz and all integral multiples thereof, when internally or line-synchronously triggered. (See page 7 for 50 Hz option and 400 Hz operation.)

AC VOLTS

Nominal Range	Overrange	Resolution
10000	.19999	10 μV
1.0000	1.9999	100 μV
10.000	19.999	1mV
100.00	199.99	10mV
1000.0	750*	100mV

*Maximum input voltage 750V RMS from 30 Hz to 10 kHz, decreasing linearly to 100V RMS at 100 kHz.

Input Impedance (all ranges): 1 megohm in parallel with <100 pF.

Sensing and Calibration: Average sensing, calibrated in RMS of sinewave

Accuracy (6 months, 23°C ±5°C):

	1V–1000V	0.1V
30 Hz	±1% rdg. ±.02% f.s.	±1% rdg. ±0.1% f.s.
50 Hz–1 kHz	±0.1% rdg. ±.02% f.s.	±0.1% rdg. ±0.1% f.s.
10 kHz	±0.25% rdg. ±0.02% f.s.	±0.25% rdg. ±0.1% f.s.
100 kHz	±1% rdg. ±0.05% f.s.	±1% rdg. ±0.5% f.s.

Temperature Coefficient (0°C to 18°C and 28°C to 50°C):
30 Hz to 1 kHz (±0.005% rdg. ±0.002% f.s.)/°C
1 kHz to 10 kHz [±(0.005 x freq. in kHz)% rdg. ±0.002% f.s.]/°C
10 kHz to 100 kHz (±0.05% rdg. ±0.002% f.s.)/°C

Settling Time (to settle within ±0.05% of full scale from full scale step input): 2.5 seconds.

OHMS

Nominal Range	Overrange	Resolution	Max. Test Current
.10000kΩ	.19999kΩ	10 milliohms	1.5mA
1.0000kΩ	1.9999kΩ	100 milliohms	1.5mA
10.00kΩ	19.999kΩ	1 Ohm	150μA
100.00kΩ	199.99kΩ	10 Ohms	15μA
1000.0kΩ	1999.9kΩ	100 Ohms	1.5μA
10000kΩ	19999kΩ	1000 Ohms	0.15μA

Max. Input Voltage: 270V DC or AC RMS (Inadvertent application of voltage to OHMS input terminals, any range.)

Configuration: True four-wire

Maximum Open-Circuit Voltage: 4.0 Volts

Accuracy (6 months, 23°C, ±1°C):
.1kΩ/1kΩ/10kΩ/100kΩ ranges: ±0.007% rdg. ±1 l.s.d.
1 megΩ range: ±0.02% rdg. ±1 l.s.d.
10 megΩ range: ±0.25% rdg. ±1 l.s.d.

Temperature Coefficient (0°C to 50°C):
.1kΩ/1kΩ/10kΩ/100kΩ ranges: (±0.002% rdg. ±0.0004% f.s.)/°C
1000kΩ range: (±0.005% rdg. ±0.0004% f.s.)/°C
10000kΩ range: (±0.02% rdg. ±0.005% f.s.)/°C

Settling Time (to settle to within ±0.01% of final reading).
.1kΩ/1kΩ/10kΩ/100kΩ ranges: 0.1 sec.
1000kΩ range: 0.4 sec.
10000kΩ range: 3.1 sec.

Settling Time in seconds for any resistance: 0.1 + 0.3 x Resistance in Megohms.

EXAMPLES:
.1kΩ/1kΩ/10kΩ/100kΩ, settles in 0.1 sec. or less.
1 megohm settles in 0.4 sec. or less.
10 megohms settles in 3.1 sec. or less.

DC/DC & AC/DC RATIO

Selected Range	Nominal Range	Overrange	Actual Display†
0.1	±.010000:1	±.019999:1	±.19999
1	±.10000:1	±.19999:1	±1.9999
10	±1.0000:1	±1.9999:1	±19.999
100	±10.000:1	±19.999:1	±199.99
1000*	±100.00:1	±199.99:1	±1999.9

*Maximum signal input voltage 1000V
†Displayed ratio is 10 times true ratio

Voltage Range:
Input Signal: 0 to ±1000V (DC or AC peak)
Reference Signal: +1V to +11V

Accuracy:
DC/DC: 24 hours, 23°C ±1°C: (±0.004% rdg. ±1 l.s.d.) x $\frac{10}{\text{Actual Ref. Voltage}}$

6 months, 23°C ±5°C: (±0.007% rdg. ±1 l.s.d.) x $\frac{10}{\text{Actual Ref. Voltage}}$

AC/DC: Multiply AC accuracy by $\frac{10}{\text{Actual Ref. Voltage}}$

Temperature Coefficient (0°C to 50°C, all ranges):
(±0.001% rdg. ±0.0005% f.s.) x $\frac{10}{\text{Actual Ref. Voltage}}$ /°C

Voltage Coefficient of Ratio: 0.00001% rdg./Volt of input signal.

Reference Input Impedance: 100kΩ

Common-Mode Rejection Ratio: } Same as in DC Volt mode
Normal-Mode Rejection Ratio: } (applies to signal channel only)

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DIGITAL DATA OUTPUTS

Logic Levels (DTL/TTL Compatible) Logic ONE: >+2.4V
Logic ZERO: <+0.4V sink for 4mA

Data: 17 lines; 1-2-4-8 BCD coded: positive true.

Polarity: 1 line; ONE = positive; ZERO = negative.

Range: 7 lines (6 ranges plus AUTORANGE indication); range in use = ZERO; all others = ONE.

CONTROL/STATUS INTERFACE

Logic Levels: same as for digital outputs.

Ready: 1 line; end of conversion is signalled by transistion from ZERO to ONE. (ZERO level indicates BUSY – i.e., that conversion cycle is active).

Sample Integration (P2): 1 line; transition from ZERO to ONE indicates that integration of input signal is over (end of P2)

Data Valid: 1 line; ONE = correctly ranged

External Trigger Input: 1 line; a positive pulse of 2.4V, with a pulse width of >1μsec and <16 msec will initiate a READ command. This command initiates a complete TRI-PHASIC® measurement cycle In the external trigger mode, that reading is then held in the output data register until the next trigger pulse is received.

Hold: 1 line; applying logic ZERO inhibits internal trigger.

Range Selection/Status: 7 lines; In remote programming mode, range is selected by grounding the appropriate line through switch contacts, grounded transistor*, or logic LOW*. In front panel local control mode, a LOW level indicates the range scale (or autorange) in use for the conversion. An 8th line, Range SEL serves as an external flag (0 denotes local mode not selected).

Mode Selection/Status: 4 lines; DCV, ACV, Ohms or Ratio is selected in remote programming mode by grounding of appropriate line through switch contacts, grounded transistor*, or logic LOW*. In front panel local control mode, a LOW level indicates the function in use. A 5th line, Mode SEL serves as an external flag (0 denotes local mode not selected).

**"ACTIVE" control methods must utilize open collector structures.*

ENVIRONMENTAL AND PHYSICAL CHARACTERISTICS

Input Power: 105V to 125V AC (or 210V to 250V AC) switch selectable (see rear-panel photograph, page 2) at nominal line frequencies of 50 Hz, 60 Hz, or 400 Hz – see page 7 for details. Power requirement is less than 15 Watts.

Temperature Ranges:
Operating: 0°C to +50°C
Storage: −25°C to +80°C

Humidity:
80% RH max, 0°C to +40°C
70% RH max, +40°C to +50°C

Overall Dimensions: 3½" high, 8½" wide, and 12" deep, including panel, controls and connectors.

Weight: 8 lbs., net, 14 lbs. packed for domestic shipment.

Stand: Adjustable, removable, tilt-up stand provided for best viewing in bench use. See page 7 for rack mounting options.

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1.4 SCOPE OF INSTRUCTION MANUAL

This manual contains complete instrument description, operating procedures, principles and theory of operation, maintenance procedures, replaceable parts lists, and reference schematics for the Model 3400, and such material is divided conveniently into 3 main parts so that Systems Engineers, Operating (Programming) personnel, and qualified Maintenance and Repair technicians may find the information appropriate for their responsibilities quickly and without having to wade through useful, but nonessential data.

Part I

Chapter 1: General Instrument Description and Performance Specifications

Chapter 2: Operating Procedures (Instrument and System Operation)

Chapter 3: Calibration & Operator Maintenance

Part II

Chapter 4: Theory & Principles of Operation

Chapter 5: Maintenance

Part III

Chapter 6: Parts Lists

Chapter 7: Reference Schematics

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2
OPERATION

2.1 UNPACKING

Each Model 3400DMM is shipped complete in a molded foam-plastic container in an individual Data Precision packing carton, and this instruction manual is on top. Carefully unpack the instrument, noting any signs of damage to the Model 3400 or to the shipping container. Retain all damaged cartons and evidence of other damage and inform the shipping agent immediately.

Each complete shipment contains one of each of the following:

Model 3400 Digital Multimeter
(line cord attached)

5-pin Remote Input Connector, A4 (mating part for Rear Panel Input)

Instruction Manual

Final Acceptance Test Data Sheet

Certificate of Conformance

Warranty Card

Fill in and return the Warranty Card.

2.2 PREPARATION FOR USE

Each Model 3400DMM has been tested, calibrated, burned-in, and re-calibrated before shipment. It is ready for use when power is connected and will deliver specified performance after a 30-minute warmup. No further calibration should be necessary; no zeroing is required, and no adjustment for it has been provided.

Instructions for connecting and operating the Model 3400DMM are contained in this chapter, and they should be read carefully before using your multimeter.

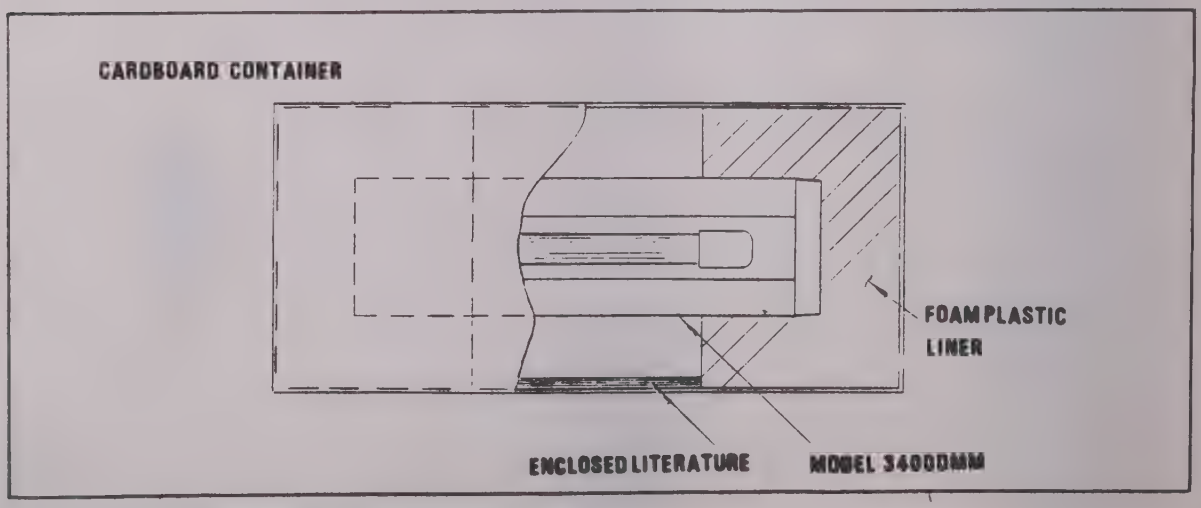

Fig. 2-1. Model 3400DMM, Shipping configuration

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WARNING:

Binding posts at the front panel are paralleled with corresponding terminals at the real panel. Signal voltages may be present at the front panel, therefore, and extreme caution should be exercised in handling front panel controls.

Table 2-1

FRONT PANEL CONTROLS AND INDICATORS (FIG. 2-2)

NOTE

Complete operating instructions follow the description of controls and indicators.

Fig. Ref.	Control/ Indicator	Description	Function
1.	DC	Push switch	Selects DC voltage measurement mode of DMM operation. Is interlocked with other modes so that it is pushed out upon selection of another mode.
2.	AC	Push switch	Selects AC voltage measurement mode of DMM action. Is interlocked with other modes so that it is pushed out upon selection of another mode.
3.	k Ω	Push switch	Selects resistance measurement mode of DMM operation. Is interlocked with other modes so that it is pushed out upon selection of another mode.
4.	RATIO	Push-push switch	Selects RATIO measurment mode in conjunction with the voltage select
5.	Vx (J2,J3)	Two 5-way binding posts	Connection for input voltage, AC or DC, or resistance.
6.	Rx (J1,J4)	Two 5-way binding posts	Current source and sink terminals for resistance connection. Connection for voltage ratio reference input.
7.	GUARD (J5)	One 5-way binding post	External connection to guard shield.
8.	DATA DISPLAY	7-segment LED indicators	Displays digital readout for a maximum of 19999. Decimal point is selected automatically and appears in the appropriate location to indicate value of a direct reading. Sign is displayed automatically when in DCV or DC/DC measurement mode.

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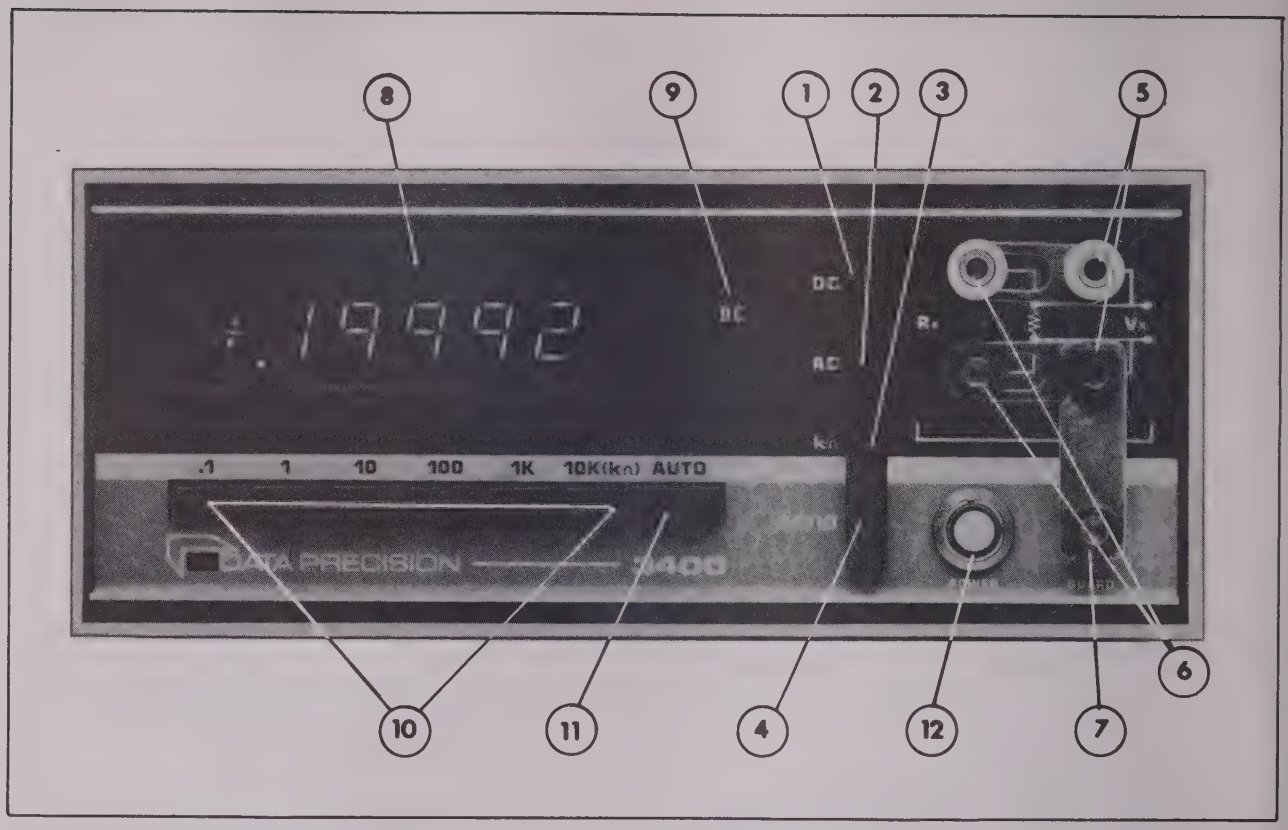

Fig. 2-2. Model 3400DMM, Front Panel Controls and Indicators

Fig. Ref.	Control/ Indicator	Description	Function
9.	ANNUNCIATORS	4 LED elements	Indicate selected measure mode
10.	RANGE DC .1 1 10 100 1K 10k(k Ω)	Push switch for manual range selection	Selects value of full scale range to be used by DMM in measuring input. Is interlocked so that only one may be in at a time. 10K for use with kΩ function only.
11.	AUTO	Push switch for automatic range selection	Initiates DMM operation to locate range for which the input signal will be measured between 10% and 200% of full scale.
12	POWER	Push-push switch	Applies or removes source power to multimeter power supply circuit

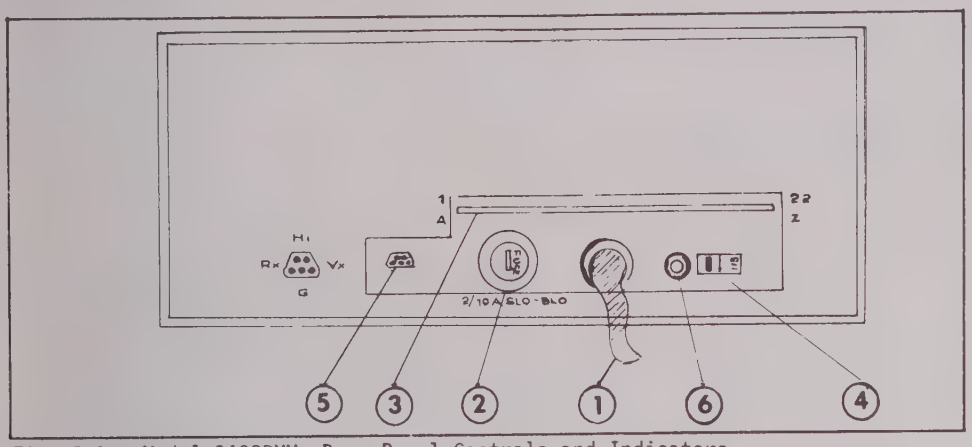

Fig. 2-3. Model 3400DMM, Rear Panel Controls and Indicators

Table 2-2
REAR PANEL CONTROLS AND INDICATORS

Fig. Ref.	Control/ Indicator	Description	Function
1.	Line Cord	3-conductor line cord	Connects 110 or 220 VAC power
2.	Fuse	Receptacle and holder	For 2/10 amp slow-blow line fuse.
3.	Remote	44-terminal connector	For remote operation/control
4.	Line Voltage Switch	Slide switch	Connects proper transformer voltage taps so that Model 3400DMM will work in user area.
5.	Input	5-pin connector	For remote input signal
6.	Binding post	Chassis ground	Ground terminal for chassis ref

2.3 LOCAL & REMOTE OPERATION

The Model 3400DMM may be operated by connecting the signal to be measured to the binding posts at the front or to a 5-pin connector on rear panel, and the measurement may be made either by operating front panel controls or by applying appropriate control signals to rear panel connector terminals. The measured value is displayed on the bright front panel LED display and is simultaneously available in parallel BCD output at terminals of the rear panel connector. The front panel display is direct-reading (Ratio X10) and includes an automatically-positioned decimal point, plus or minus polarity sign (if appropriate to the measurement), lighted annunciator to indicate the mode of measurement being made (DCV, ACV, kΩ, or Voltage Ratio); while the rear panel connector provides signal indicators of these measured characteristics. In addition, the rear panel connector provides signals to indicate when the output BCD data and polarity are valid, and the connection for applying an external trigger and for holding a previous conversion.

2.3.1 Guard Connections.

Instrument construction provides a GUARD circuit connected to the internal shield surrounding the analog and A/D sections of the instrument and isolated from any analog input or external ground. Prior to any measurement, a proper GUARD connection must be made in order to bring the internal shield as close as possible to the voltage potential of the low side of the input circuit. The GUARD connection should be made to minimize the common mode currents through the voltage measuring circuit, and it should be connected to the low side as close as possible to the voltage source. If it is not feasible to connect at the source, make the connection between GUARD and the low side of the input at the DMM front panel.

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2.4 FRONT PANEL (LOCAL) OPERATION

2.4.1 DCV Measurement

a. Connect signal inputs as shown in Figure 2-4. Observe precautions concerning maximum input and common mode voltages. See specifications, para. 1.3.

b. Select DCV mode by operating DCV pushbutton. Observe Annunciator "DC".

c. If manual ranging is to be used, select range scale for maximum resolution of input signal. Start by operating X.1 range (10uV resolution). If range scale is too low for the input signal, the conversion will result in an out-of-range display, the polarity sign remains lighted, while all digits are blanked. Select the X1 scale, and observe the display. Continue until the display indicates an in-range measurement.

d. If auto-ranging is to be used, select auto-ranging by operating AUTO pushbutton. Wait until the display is complete (no blanking) as the Model 3400DMM performs successive conversions until the proper range scale is automatically selected.

e. Read the display directly in volts with indicated polarity.

2.4.2 ACV Measurement

a. Connect input signal as shown in Figure 2-4. Observe precautions of maximum input voltage. See specifications, para. 1.3.

b. Select ACV mode by operating ACV pushbutton. Observe annunciator light "AC " in Display.

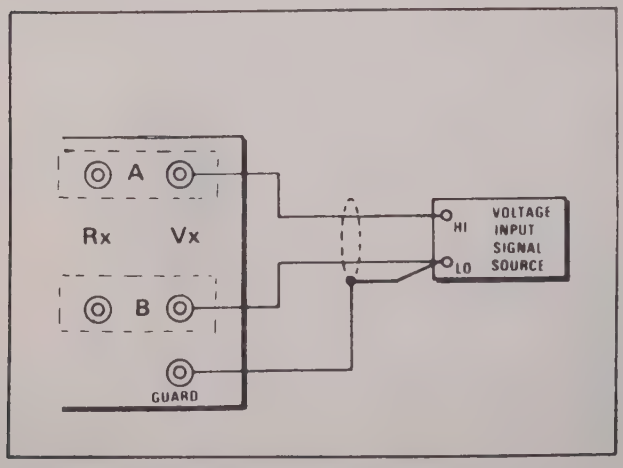


Fig. 2-4. Voltage Measurement connections

c. If manual ranging is to be used, select the range scale for maximum resolution (X.1), and observe display. If out-of-range indication is displayed (see above), select X1 range scale, and repeat until converted value is displayed.

NOTE: Polarity sign is not lighted for ACV measurements.

d. If auto-ranging is to be used, operate AUTO pushbutton and wait for in-range displayed value.

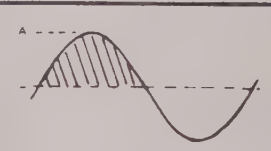
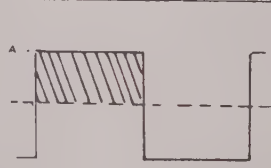
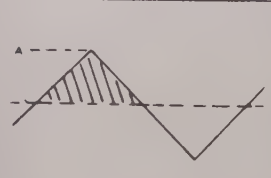
e. Read directly in RMS ACV. The displayed value is calibrated for sinewave inputs. For other than sinewave inputs, a multiplying factor may be applied, depending upon the waveshape and by using the factors shown in Table 2-3.

2.4.3 Resistance Measurement

a. Connect input resistance in one of the input configurations shown in Figure 2-5 or 2-6. Four-wire connections, if possible, provide the most accurate measurement of the unknown resistance, eliminating effects of lead length and contact resistance in the conversion. Observe precautions of maximum input voltage if "live circuits" are to be measured.

Table 2-3

MULTIPLYING FACTORS FOR AC MEASUREMENTS

WAVEFORM	AVG VALUE PER MODEL 3400	RMS VALUE	MULTIPLY DISPLAY BY
	.707A	.707A	1.0
	1.11A	1A	.901
	.555A	.577A	1.040

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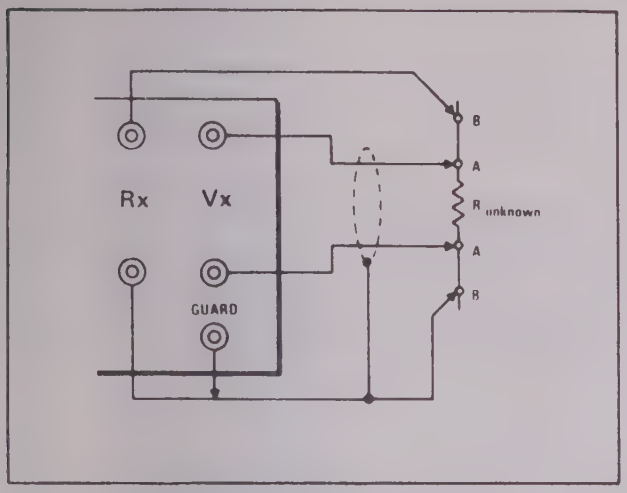

Fig. 2-5. Resistance Measurement, 4-wire

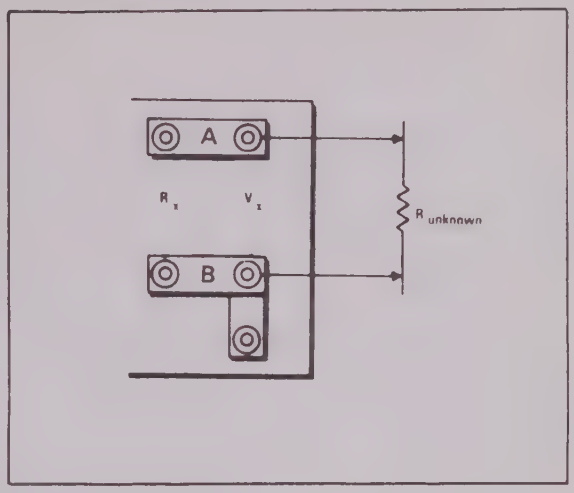

Fig. 2-6. Resistance Measurement, 2-wire

b. Select resistance measurement mode by operating kΩ pushbutton. Observe Annunciator "KΩ" in Display.

c. If manual ranging is to be used, select range scale X.1 for maximum resolution (10 milliohm). Observe display. If out-of-range indication is displayed, select X1 range scale, and continue until in-range measurement is displayed.

> NOTE: For resistance measurement, there are 6 possible range scales, as distinct from the 5 scales available for voltage measurements.

d. If auto-ranging is to be used, operate the AUTO pushbutton. Wait for in-range conversion to be displayed.

e. Read the resistance directly in kilohms.

2.4.4 Voltage Ratio Measurement

a. Connect the DC reference voltage (+1V to +11V) to the reference Rx inputs and the AC or DC "unknown" voltage to the Vx inputs as shown in Figure 2-7. Observe same precautions about the unknown input as for the ACV or DCV measurements.

b. Select voltage ratio mode by operating RATIO pushbutton. Operate proper DCV or ACV pushbutton depending upon unknown input. Observe appropriate Annunciator light in Display.

c. If manual ranging is to be used, select X.1 range scale for maximum resolution (1.00000:1). If resulting measurement is out-of-range display, select X1 range scale, and continue until in-range measurement is displayed (or overload input persists on X1000 range).

d. If auto-ranging is to be used, operate AUTO pushbutton. Wait for in-range display.

e. Read display. Divide the displayed value by 10 to obtain the measured ratio. For DC input voltages, polarity display indicates polarity of the "unknown" DCV with respect to the positive reference input.

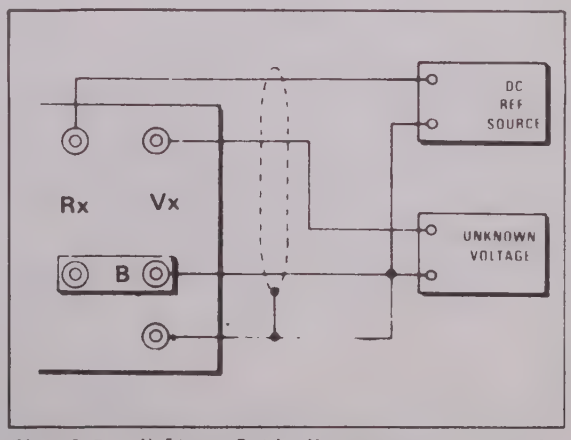

Fig. 2-7. Voltage Ratio Measurement connections

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2.5 REMOTE (PROGRAMMED) OPERATION

2.5.1 System Connections

a. Input Signals may be connected to the rear input connector as shown in Figure 2-8, noting that external system programming may be used to switch the "reference" inputs from the normally guard-shorted function to active inputs when switching from ACV or DCV to Resistance and Ratio measurements.

b. Input Control and Output Data and Status Signals should be cabled as shown in Table 2-4. A typical system connection is shown in Figure 2-9, and that illustration identifies some of the functions that may be performed by the control inputs and status outputs.

2.5.2 Remote (Programmed) Mode and Range Scale

a. Release all front-panel Mode and Range Scale selection pushbuttons so that none remains actuated, and all are in released position.

b. Check the status of the Mode $\overline{SEL}$ (pin 5) and Range $\overline{SEL}$ (pin 21). A low level at these pins indicates that all front panel switches have been released, and that these selections may be programmed externally. A high level for these $\overline{SEL}$ signals may be used to inhibit remote programming.

c. Program the desired measurement mode and range scale by applying DTL/TTL - compatible low levels to the appropriate terminals as defined in Table 2-4. Active control methods must utilize open collector structures.

2.5.3 Remote (Programmed) TRIGGER and $\overline{HOLD}$

a. Apply a low level to $\overline{HOLD}$ (pin H) to prevent internal triggering control.

b. To initiate remotely controlled conversion cycles, raise TRIGGER (F) to a positive level for at least 1usec and retain the high level for up to 16 msec. (See timing waveform of Figure 2-10.)

c. The DMM Model 3400 will complete as many conversion cycles as possible as long as TRIGGER (F) is at high level. The minimum duration of a conversion cycle is 39+2ms (600kHz clock) or 46+2ms (500kHz clock). To limit the operation to a single conversion per trigger, the TRIGGER control signal should be less than 16 msec.

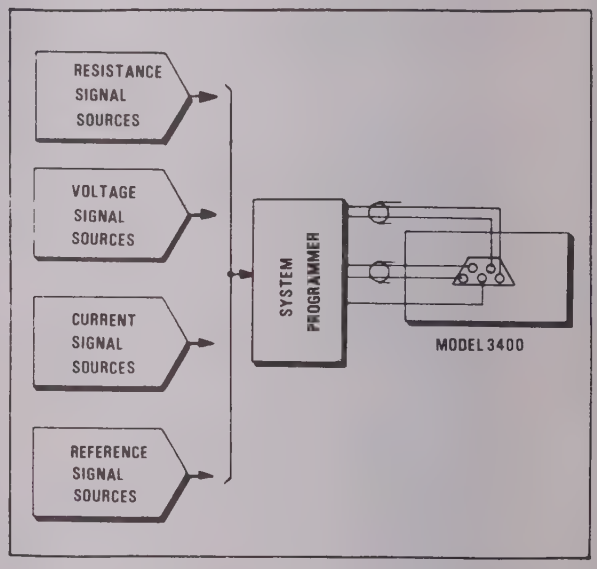

Fig. 2-8. Programming via Rear Input Connector

Table 2-4
MODEL 3400DMM REAR PANEL CONNECTOR,

Designations for DATA, STATUS,

and CONTROL signals

*	A	1	$\overline{P2}$(SAMPLE INTEG)	20	N	12	***
$\overline{AUTO}$	B	2	$\overline{RATIO}$	10	P	13	800
$\overline{X10K}$	C	3	$\overline{AC}$	8000	R	14	400
$\overline{X1000}$	D	4	$\overline{DC}$	4000	S	15	200
SIGN VALID	E	5	$\overline{SEL}$(MODE)	2000	T	16	100
TRIGGER	F	6	KΩ	1000	U	17	$\overline{X100}$
$\overline{HOLD}$	H	7	READY(EOC)	8	V	18	$\overline{X1}$
SIGN	J	8	10,000	4	W	19	$\overline{X.1}$
DATA VALID	K	9	GND(DIG)	2	X	20	$\overline{X10}$
*	L	10	80	1	Y	21	$\overline{SEL}$(RANGE)
$\overline{READ}$	M	11	40	*	Z	22	*

* Not Connected
*** Not to be used

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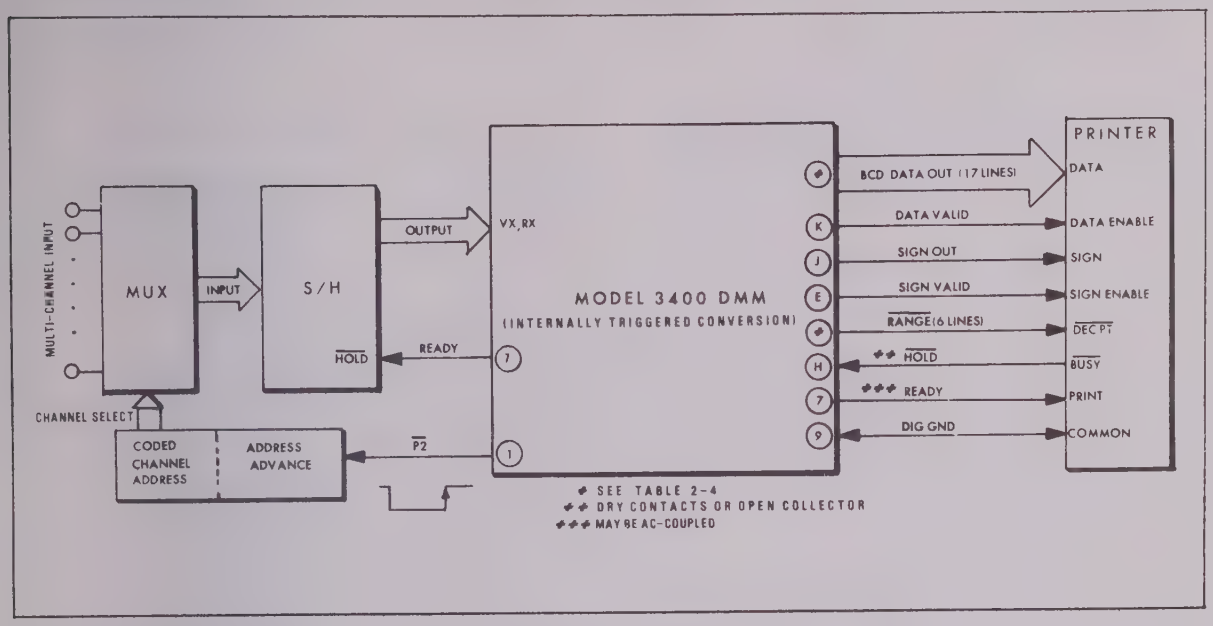

Fig. 2-9. Typical remote system operation of MODEL 3400DMM

2.6 MIXED LOCAL (FRONT PANEL) AND REMOTE (PROGRAMMED) OPERATION

Local and remote operation of Model 3400DMM are not mutually exclusive. That is, some multimeter functions may be controlled by remote programming while the others are controlled by front panel operation. For example, measurement mode and range scale selection may be accomplished by front panel (local) operation, while conversion start is controlled by external triggering (remote). Or, for another example, mode selection may be made by front panel control while range scale selection simultaneously is made via system program control (or vice-versa). When a selection is made at the front panel, the rear connector control line becomes a status line and indicates the selection by appearance of a DTL/TTL - compatible low level on the line. In all combinations of local and remote control, however, the Data Output and conversion status signals are available at the rear connector as well as by visual display on the front panel.

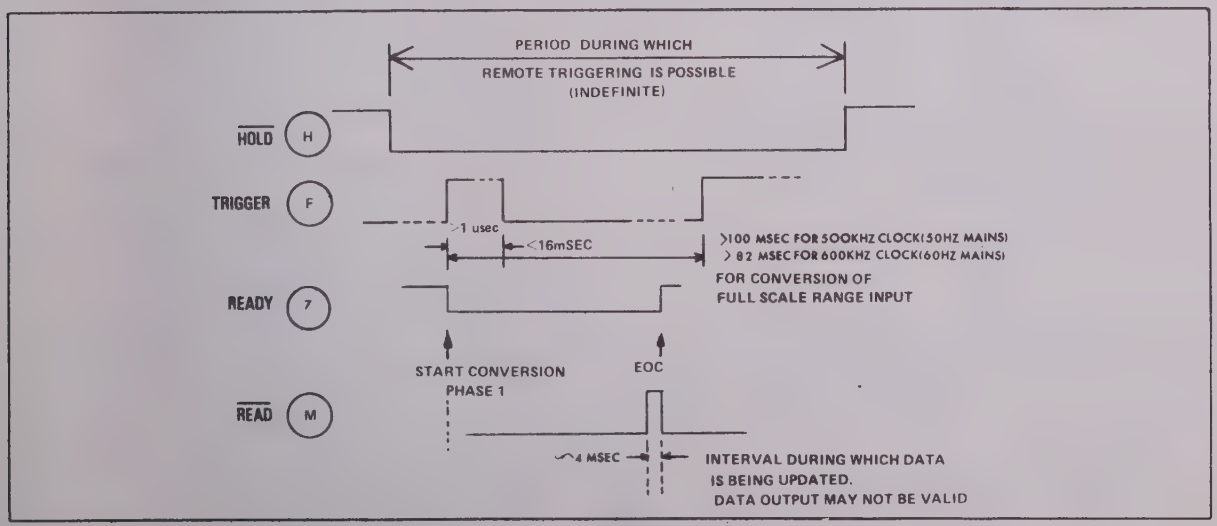

Fig. 2-10. Trigger generating waveforms

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3
CALIBRATION

Data Precision Model 3400 Digital Multimeter is an extremely precise and stable instrument. Its 6-month specified accuracy should last for longer than the specified period. It is advisable to check the instrument periodically. When doing so, follow all procedures carefully and observe all precautions.

3.1 CALIBRATION VERIFICATION

Data Precision recommends establishing and maintaining a performance history log of the Multimeter. Transfer the certified factory performance test data as the initial entry. In order to have a locally available test performance for comparison, it is suggested that the instrument be tested against an available standard as soon as it is unpacked and the test results be recorded at that time. The instrument should be checked thereafter every six months.

3.2 PRELIMINARY SET UP CONDITIONS

a. Establish a solid ground connection from the case to the power source ground. If the third wire of the three-wire power cord does not carry through to main power ground, ground the meter case with a clip lead attachment to the ground binding post at the rear panel.

b. Accuracy of standards used to calibrate the multimeter should be verified before recalibrating the instrument. Errors of

Table 3-1 TABLE OF CALIBRATING EQUIPMENT

Procedure	Type/Model No.	Performance Specs/Acc. Require.
DC Volts	COHU/Model 355	1V range ± .001% rdg 10V range ± .001% rdg + 5 uV 100V range ± .001% rdg + 20 uV 1000V range ± .001% rdg + 40 uV
AC Volts	HP/Model 745A HP 746A	1mV to 100V: 50Hz-20kHz ± .02% rdg ± .002% range + 10uV 20kHz-100kHz ± .05% rdg ± .005% range + 50uV 100V to 1000V: 50Hz-20kHz ± .04% rdg 20kHz-50kHz ± .08% rdg
Resistance	JULIE/DMR-105A (.001%) JULIE/NB-106-1M (.0015%) JULIE/NB-107-10M (.003%)	1 kilohm to 10 megohm ± .001% in decades
Normal Mode Rejection	Data Precision Counter Model 5740	600.000 kHz ±0.2 Hz 500.000 kHz ±0.2 Hz

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standards should be no worse than 20% of the tolerances specified for the multimeter.

3.3 CALIBRATING EQUIPMENT TABLE

The equipment in the table is recommended for use in the calibration procedure. Substitute units may be employed provided they meet the specified accuracy characteristics.

3.4 ACCESS TO CALIBRATION ADJUSTMENTS (FIG. 3-1)

All calibration adjustments are accessible after the meter top cover is removed. The calibration components (trim pots & trim caps) are mounted on the main circuit board; those in the analog circuit may be reached through openings provided in the GUARD shield, while the single digital circuit adjustment (trim capacitor) is located adjacent to the Guard among the digital circuit components. A summary table of calibration procedures is located on the inside top cover.

> CAUTION
>
> Do not remove the Guard during Calibration Process.

3.5 CALIBRATING SEQUENCE

All adjustments are made with the Model 3400 in operation. Perform the calibration in the following sequence (after 30-minute warmup):

a. Clock frequency

b. Zero baseline

c. Reference voltage

d. Buffer X10 Gain control

e. Input divider network

f. AC frequency response

3.5.1 Clock Frequency Adjustment

a. DMM normal mode rejection is optimized (with respect to rejecting line frequency noise) by adjusting the clock frequency so that 10,000 counts of the clock is an integral multiple of line frequency cycles. Thus, for a 60-cycle line frequency, the clock has been factory-set for 600 kHz; while for 50-cycle or 400 cycle line frequency the clock circuit is tuned for 500 kHz. The clock may be field calibrated for line frequencies other than the standard 50, 60, or 400 Hz, or may be recalibrated to the 500 kHz or 600 kHz values by adjustment of C13 (see Figure 5-1.).

b. Use the frequency meter (5740) to determine the value of line frequency.

c. Using the frequency meter with X20 ATTEN, measure the frequency between the R4-R5 junction and DIG GND. Adjust C13 for the appropriate value of clock frequency as determined in step b. above.

3.5.2 Zero Baseline Adjustment

a. Select DCV measuring mode.

b. Select X10 range scale.

c. Short input with a jumper between HI and LO of Vx at input terminals.

c. Adjust R23 for a display of 00.000 and a polarity sign that flickers between plus (+) and minus (-).

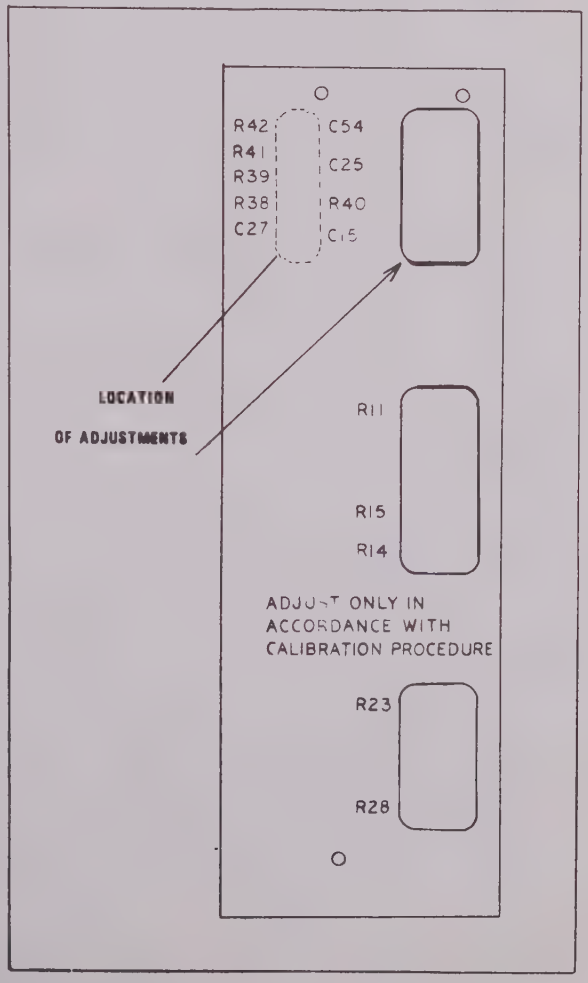

Fig. 3-1. Access to Calibration adjustments

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3.5.3 Reference Voltage Adjustment

a. Apply -1.90000 VDC to input Vx.

b. Select Range Scale X1.

c. Adjust R15 for display of -1.9000 .

3.5.4 Buffer X10 Gain Adjustment

a. Apply -.190000 VDC to input Vx.

b. Select range scale X.1.

c. Adjust R28 for display of -.19000.

3.5.5 Input Divider Network Adjustments

a. Select kΩ measuring mode.

b. Select range scale X1.

c. Connect resistance of 1.00000 kΩ to input terminals using the 4-wire input configuration as shown in Chapter 2.

NOTE: Any resistance, known to a tolerance of ± .05 Ω may be used.

d. Adjust R42 for display of 1.0000, or to the value of the known resistance.

e. Select range scale X10.

f. Apply resistance of 10.0000 kΩ (or accurately known comparable value, ±0.5 Ω).

g. Adjust R41 for display of 10.000 or the accurately known value.

h. Select range scale X100.

i. Apply resistance of 100.000 kΩ, or accurately known comparable value ±5 Ω.

j. Adjust R40 for display of 100.00 or accurately known input value.

k. Select range scale X1K.

l. Apply resistance of 1000.00 Ω, or accurately known comparable value ±50 Ω.

m. Adjust R39 for display of 1000.0, or the accurately known input value.

n. Select DCV measuring mode.

o. Select range scale X10.

p. Apply +19.0000 VDC input signal.

q. Adjust R38 for display of +19.000.

3.5.6 AC Frequency Response Adjustments

a. Select ACV measuring mode.

b. Select range scale X1.

c. Apply 1.9000 VRMS sinewave at 200 Hz to input.

d. Adjust R11 for a display equal to applied input.

e. Select range scale X1K.

f. Apply 200.0 VRMS sinewave at 20 kHz to input.

g. Adjust C15 for a display value equal to applied input value.

h. Select range scale X100.

i. Apply 190.00 VRMS sinewave at 20 kHz to input.

j. Adjust C54 for a display equal to applies input value.

k. Select range scale X10.

l. Apply 19.000 VRMS sinewave at 20 kHz to input.

m. Adjust C25 for a display equal to applied input value.

n. Select range scale X1.

o. Apply 1.9000 VRMS sinewave at 20 kHz to input.

p. Adjust C27 for a display equal to applied input value.

3.6 POST-CALIBRATION

As calibration is completed, enter date below and initial. Turn off power. Reassemble unit by replacing cover.

(See Table 3-2.)

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Table 3-2
CALIBRATION RECORD

Date	Calibrated By (Name)	Date	Calibrated By (Name)

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4
PRINCIPLES & THEORY OF OPERATION

4.1 GENERAL, CHAPTER PLAN

This Chapter is divided into two main parts. The first part briefly describes the operation of the Model 3400DMM in terms of functional blocks which are grouped into major subsystems. The second part contains more detailed performance descriptions with reference to circuit schematics. This second part is intended to provide repair technicians with circuit descriptions as background for later troubleshooting and repair operations, and may be omitted without detracting from an understanding of the Model 3400DMM performance.

4.2 SYSTEM BLOCK DIAGRAM (FIGURE 4-1)

As shown in Figure 4-1, Model 3400DMM consists of six operating subsystems and a power supply subsystem. The analog A/D and input conditioning subsystems are isolated from the others by opto-isolators and relays for maximum system flexibility and noise-free performance. In addition the power supplies for analog and digital circuits are decoupled by appropriate transformer shielding to maintain the integrity of the analog-digital isolation.

4.2.1 Signal Conditioning Subsystem.

The signal conditioning subsystem, under control of front panel selectors or rear panel signals, scales the input signal to 1 volt for nominal full scale (2 volts, including 100% overrange). The signal conditioning subsystem includes the precision voltage divider network for DC signals of 1 volt or more, and the necessary AC/DC rectifier and scaling for rms-to-output scale factor conversion of input AC signals.

Inputs of less than 0.1 volt are signal conditioned for the nominal 1 volt full scale, but are scaled by changing gains in the analog A/D subsystem. The control signal for this operation is transmitted to the analog section via opto-isolator to maintain the analog-digital isolation when in the X.1 range scale. (Figure 4-1.)

4.2.2 Mode & Range Control Subsystem.

The mode and range control subsystem translates the front panel switch selections or rear panel signal inputs to the relay-operated precision network and input configuration switch contacts required for the signal conditioning subsystem. This subsystem also includes the digital logic programming that responds to the out-of-range signal from the digital programming subsection so that when in auto-ranging operation, the range selection operates as required to select the appropriate range for the input signal.

4.2.3 Analog A/D Conversion Subsystem.

The isolated analog A/D Conversion Subsystem, under program control provided by the Digital Programming Subsystem, translates the conditioned analog input to a proportional time interval indicated by the EOC output of a binary comparator. The A/D conversion is accomplished by the unique Data Precision Tri-Phasic™ 3-phase conversion technique that (1) auto-zero's the circuit to store an off-zero compensation, (2) integrates the conditioned input for 10,000 clock counts, and (3) integrates a precise reference of opposite polarity until the charge on the integrating capacitor is removed. The polarity of the conditioned input is indicated by the comparator output at the end of the second phase and transmitted via opto-isolator to the digital programming subsystem. The end of conversion (EOC) is similarly transmitted at the end of phase 3.

4.2.4 Digital Programming Subsystem.

The Digital Programming Subsystem, in a cycle enabled by internal or external trigger, generates the phase control signal levels for 3-phase A/D conversion, including the selection of proper polarity of the reference from the Isopolar™ reference circuit. This subsystem also includes the counter and logic circuitry that translates the time interval from the A/D into

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multiplexed BCD data codes (parallel by bit, serial by digit) for the Display Subsystem and directly for the Output Subsystem. It also provides the control signals for the decimal point and the polarity in the Display Subsystem.

If the Digital Programming Subsystem does not receive an EOC indication within 20,000 counts of the start of the reference integration phase, it generates out-of-range control signals that blank the display, and when in auto-range, initiate a programmed range-scale change to select the suitable range of at least 10% of full scale; or, if already at maximum range scale, maintains the out-of-range blanking indication.

4.2.5 Display Subsystem.

The Display Subsystem translates the multiplexed BCD data from the Digital Programming Subsystem into a 7-segment LED display of 4 full decades and MSD "1" values, lights the selected decimal point, polarity sign (if DCV or DC Ratio), and annunciator. If the signal is out-of-range, the Display responds to the blanking control by blanking all digits; the decimal point, and polarity sign (if appropriate) remain lighted.

4.2.6 Input Control & Output Status Subsystem.

The Input Control and Output Status System routes DTL/TTL - compatible signals in to and out of the Model 3400DMM. Remote system programming may select the measurement function, the range scale (or autoranging), initiate up to 12/sec (for max. input to 60 Hz instruments), or hold measurements indefinitely. Output data in BCD format are available in parallel output lines, and status lines indicate the range scale (locating the decimal point), the polarity (for DC signals or DC RATIO), when the data is valid (not overload, or while range selecting in AUTO), and when polarity is valid (for ± DCV inputs). In addition, when in local (front panel) control, the output lines indicate the mode and the range scale selected, and when no selection of either has been made at the front panel.

4.2.7 Power Supply Subsystem.

Model 3400DMM may be sourced from either 105 to 125 VAC or 210 to 250 VAC at nominal line frequencies of 50, 60, or 400 Hz. It develops the necessary analog and digital power supplies in the Power Supply Subsystem. The analog and digital supplies are isolated for optimum noise-free performance and versatile system applications.

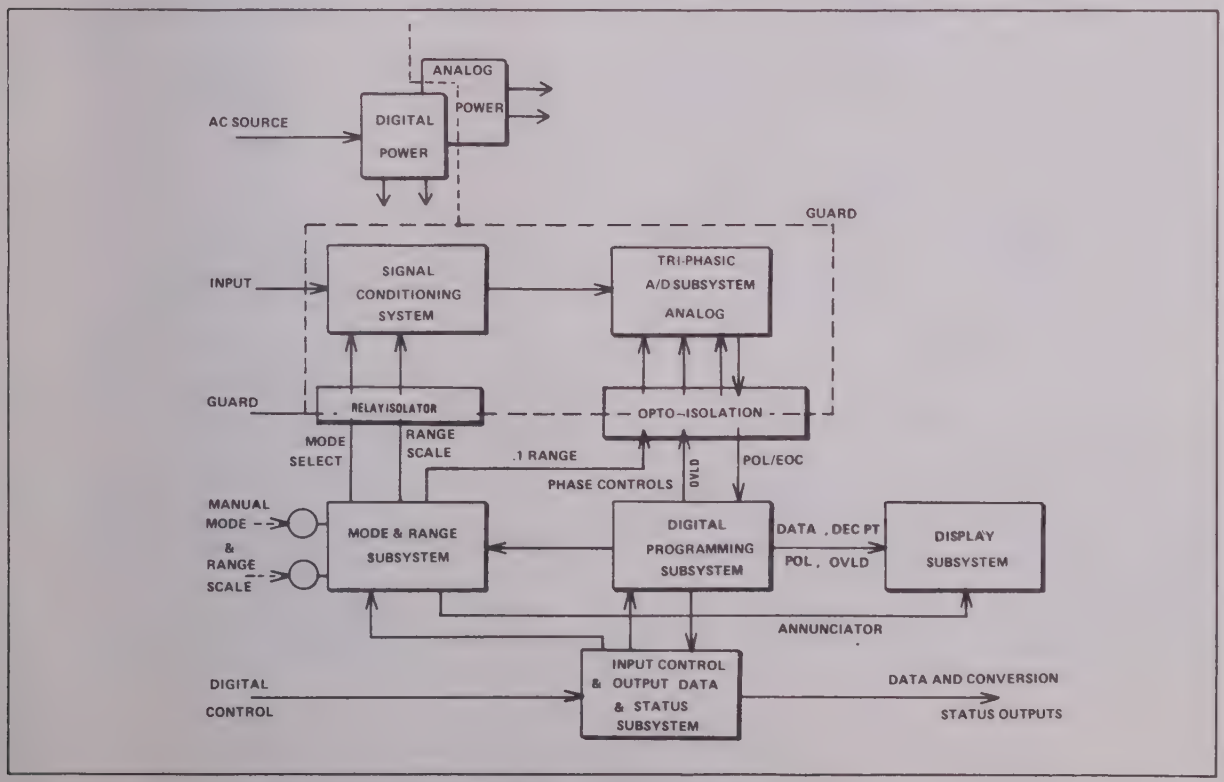

Fig. 4-1. Model 3400DMM System Block Diagram

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4.3 SYSTEM TIMING & WAVEFORMS (FIGURE 4-2)

Each conversion of conditioned input to digital display and signal outputs is initiated by a TRIGGER command that is generated internally, or that may be applied through the rear connector by the system programming. The conversion is completed in less than 80 milliseconds (60 Hz instruments) for maximum input signal variations between conversions. Each conversion is complete in itself, independent of previous conversions, and auto-zeroed for a minimum of 10,000 clock counts at the start of each conversion.

Application of a TRIGGER command (internal or external), enables the Digital Programming Subsystem to generate or continue a Phase 1 control signal (P1) that starts or continues the auto-zeroing phase of the Tri-Phasic A/D conversion after completion of any conversion in process. This lasts for at least 10,000 counts of the crystal-controlled clock, after which the programmer generates a Phase 2 control signal (P2), for the input integration phase. The Phase 2 duration is also 10,000 counts, after which the programmer generates the selection of the polarity of the reference, issuing a $P3^+$ of $P3^-$ control level (for positive and negative inputs, respectively), for the reference integration phase. Phase 3 ends with the generation of an EOC signal through the opto-isolator Z29 when the comparator senses a zero-voltage level in the A/D converter. If the EOC signal does not appear within 20,000 counts after the start of phase 3, the Data valid line will go low and the display will be blanked.

Figure 4-2A illustrates the timing relationships for an input within full scale range (less than 20,000 counts in Phase 3) among the control and status signals. Figure 4-2B shows the change in waveforms for an out-of-range signal (over 20,000 counts).

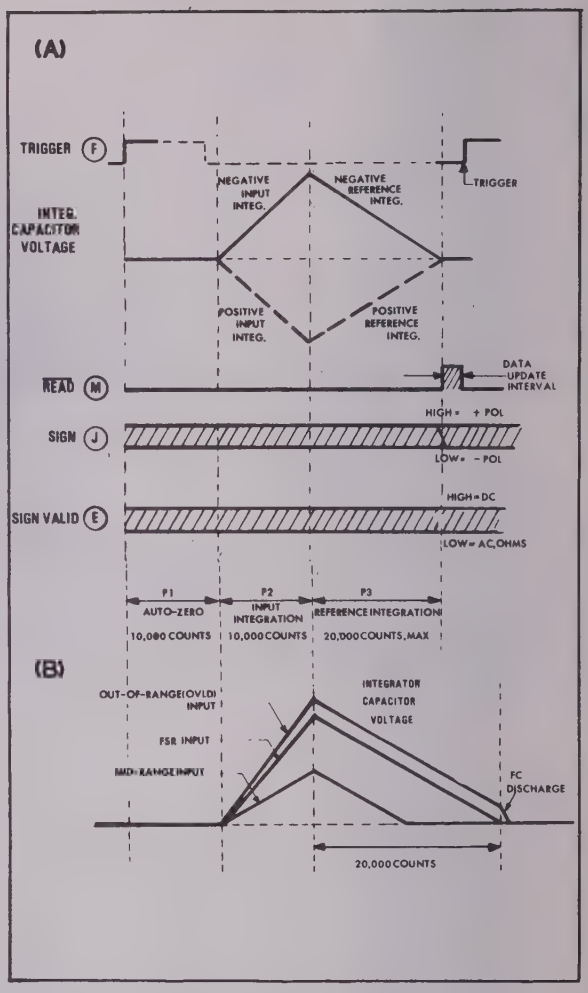

Fig. 4-2. System Timing Diagram
(A) In-Range input; (B) Out-of-Range input.

4.4 SIGNAL CONDITIONING

4.4.1 DCV Measurement Mode (Figure 4-3).

When in DCV mode, input DC signals are connected to the input attenuator network through contacts of mode relays "KM". Figure 4-3 illustrates the connections for a X100 input range. Note that the signal is passed through without attenuation in the X1 range; the scaling for X.1 range is accomplished in the A/D converter block and will be described in detail later.

When attenuation is required (X10, X100, X1000), the input is terminated in 10 megohms, while in the other range scales (X.1 and X1), the input impedance is essentially that of the analog input stage, or 1000 megohms, minimum.

Parallel capacitances shown schematically in Figure 4-3 are not active in DCV signal conditioning. They are used to calibrate the network for ACV signal conditioning as described in para. 4.4.2.

The resulting attenuator actions of the KR relays for voltage and resistance modes are

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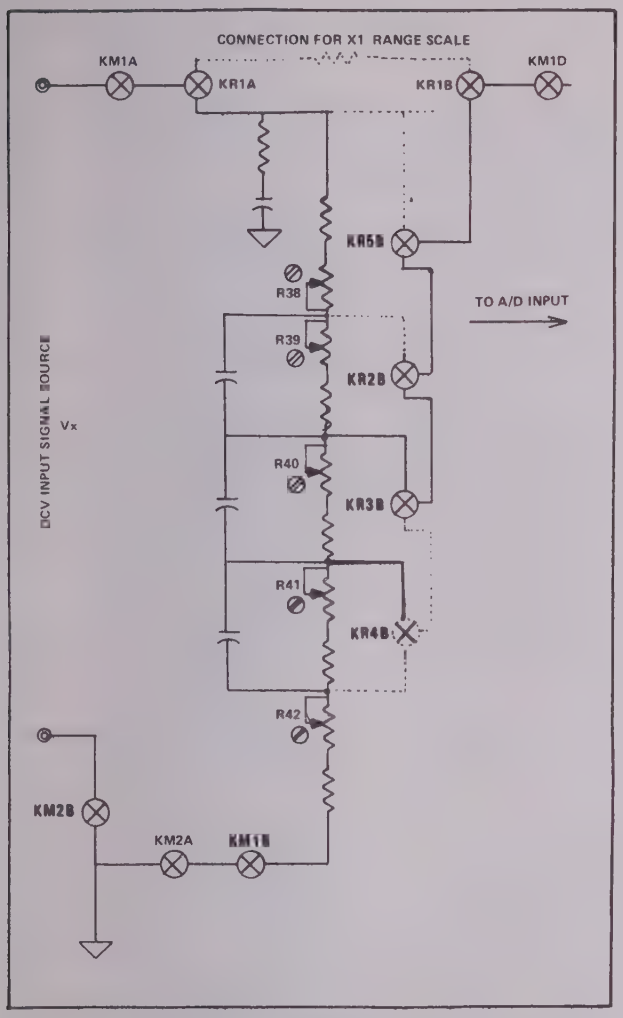
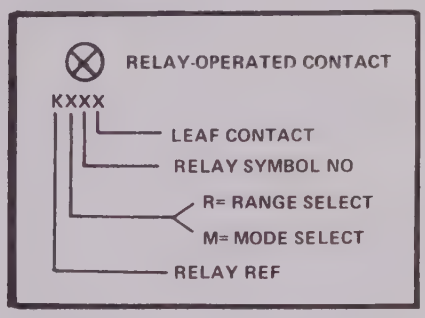


Fig. 4-3 Input Divider Network, simplified schematic for X100 Range



Graphic Symbol Conventions

summarized in Table 4-1. The table also indicates the appropriate decimal point activation controlled by the relay action. Note that the 10K range scale is useful only when in resistance measurement mode.

4.4.2 ACV Measurement Mode Signal Conditioning (Figure 4-4).

When in ACV mode, the input AC signal is connected to an active broad band attenuator configured by the action of the mode relay and the range relay contacts. The mode relay (KM) contacts connect the precision attenuator in the feedback path of an operational amplifier, providing the instrumentation for range scale attenuation, as shown in Figure 4-4. The attenuated AC signal is then rectified and filtered so that 2.22X the average half-period value of the attenuated input AC signal is scaled for nominal 1.0VDC full scale input to the A/D converter. This scaling permits the output

Table 4-1

Range Relay Logic Truth Table

KΩ

RANGE	KR1	KR2	KR3	KR4	KR5
X.1	0	1	1	1	0
X1	0	1	1	1	0
X10	0	1	1	0	0
X100	0	1	0	0	0
X1000	0	0	0	0	0
X10K	0	0	0	0	1

D.C. - RATIO

RANGE	KR1	KR2	KR3	KR4	KR5
X.1	0	0	0	0	0
X1	0	0	0	0	0
X10	1	0	0	0	0
X100	1	1	0	0	0
X1000	1	1	1	0	0
X10K	1	1	1	0	0

A.C. - RATIO

RANGE	KR1	KR2	KR3	KR4	KR5
X.1	0	0	0	0	0
X1	0	0	0	0	0
X10	0	1	0	0	0
X100	0	1	1	0	0
X1000	0	1	1	1	0
X10K	0	1	1	1	0

Decimal Point Location to Left of (Note 1)
D5
D4
D3
D2
D1
To right of D1

Note 1: D1 is least significant digit, D5 is MSD "1".

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display to be read directly in RMS units for sinewave inputs. Refer to the table in Chapter 2 for conversion factors to translate output data to RMS values of other waveforms (Table 2-3).

4.4.3 Resistance Mode Signal Conditioning (Figure 4-5).

Model 3400DMM utilizes the dual-slope operation of the Tri-Phasic A/D conversion technique to make accurate and ultra-stable resistance measurements. The unknown resistance is connected in series with a relay-selected precision range scale-resistance and in series with a known voltage source as shown in the simplified schematic of Figure 4-5A. During Phase 2 of the Tri-Phasic conversion, the voltage developed by the resistance connected between HI and LO input terminals is the input for the unknown integration phase through P2-operated switch Q13. Then, in Phase 3, the voltage across the selected range scale resistor, which has charged capacitor C39, is the input for the reference integration phase. The displayed value may then be read directly in kilohms, and a maximum reading of 19,999 kilohms (20 megohms) is available on the sixth range scale (X10K).

This method of resistance measurement obtains its high accuracy, in part because:

a. The developed voltages by the unknown resistance and the precision range resistor are generated by the same current in the conditioning circuitry.

b. The 4-wire configuration eliminates the effects of the contact resistances in the measurement of resistor-generated voltages.

4.4.4 Ratio Measurement Signal Conditioning (Figure 4-6).

When in Ratio Mode of operation, the internal reference is replaced with the applied reference voltage for use during phase 3 of the Tri-Phasic A/D conversion. Signal conditioning of the input is accomplished in the same general manner as when making DCV and ACV measurements directly. The relay operation is modified to account for the required signal conditioning of the reference input which may be as much +11VDC, and therefore is attenuated by a factor of 10 before being applied in Phase 3.

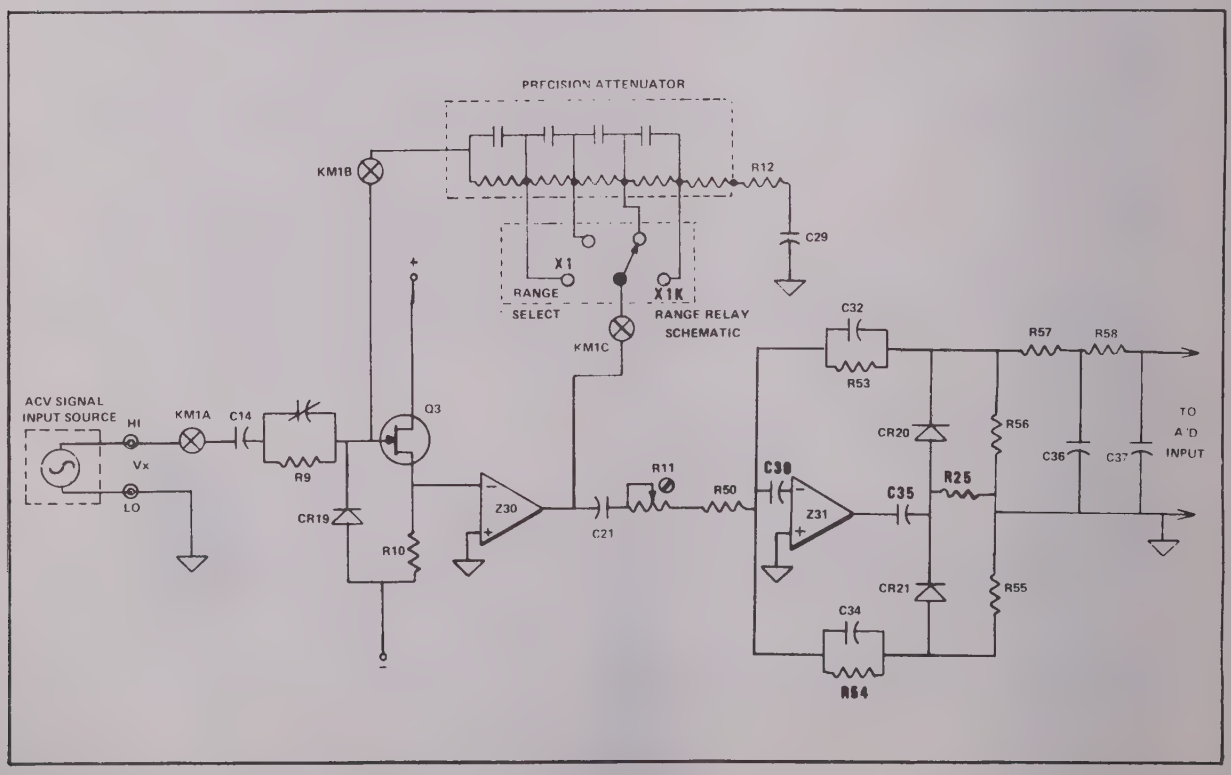

Fig. 4-4. AC Input Signal Conditioning, simplified schematic

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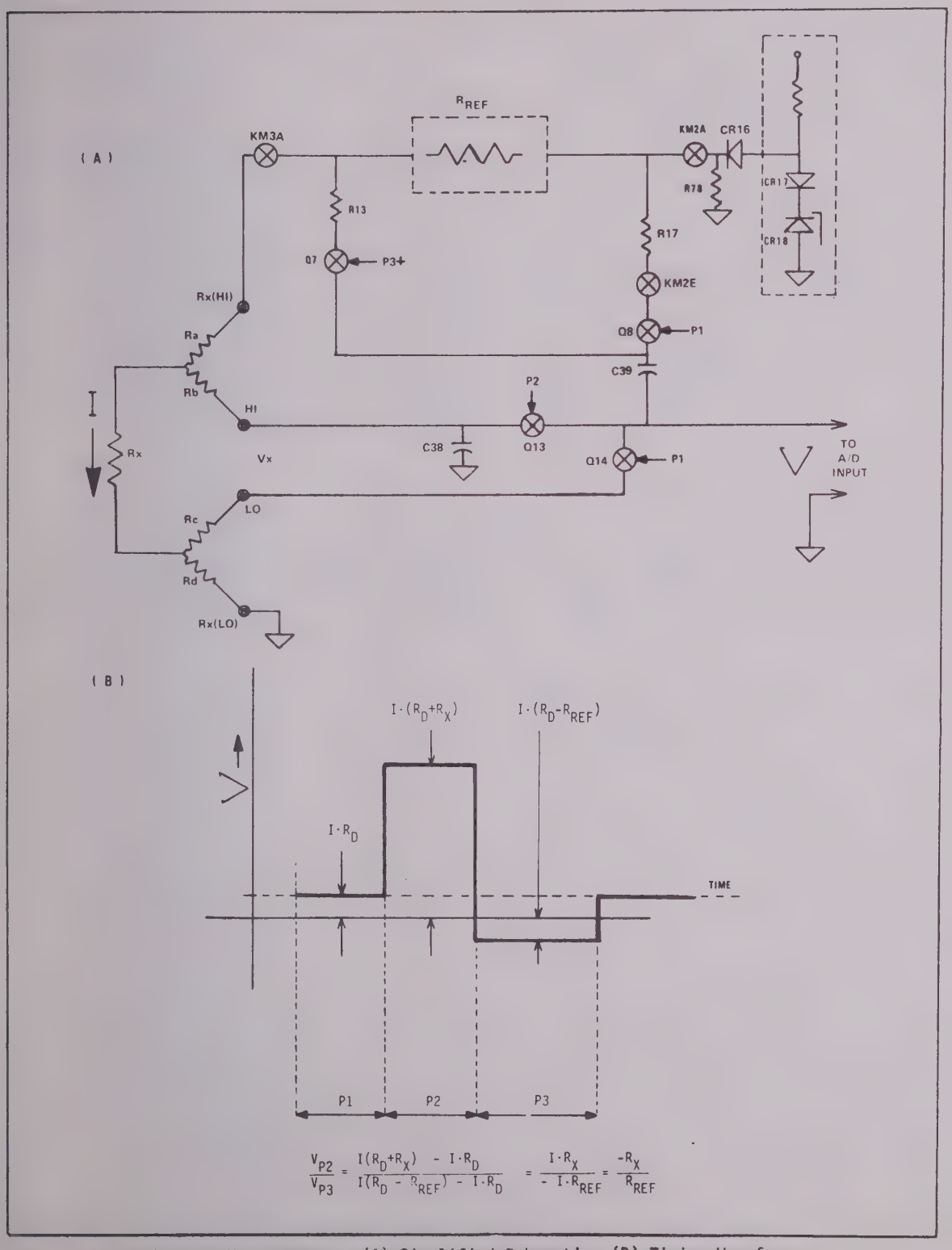

Fig. 4-5. Resistance Measurement. (A) Simplified Schematic (B) Timing Waveforms

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The division by 10 of the reference results in a display value which is 10 times greater than actual, and requires a compensating manual division by 10 of the displayed result to determine the actual measured ratio.

4.5 TRI-PHASIC A/D CONVERSION (Figure 4-7)

As explained in the introductory material of Chapter 1, the 3 phases of a Tri-Phasic A/D conversion consist of: Phase 1, during which the voltage-generating drifts are sensed and stored for subsequent compensation; Phase 2, during which the conditioned input (1 volt full scale) is integrated for a fixed time; Phase 3, during which a precision reference voltage is integrated for a time proportional to the magnitude of the conditioned input. Figure 4-7 illustrates the manner in which this technique is instrumented in Model 3400DMM.

As shown in Figure 4-7, the conditioned input is connected to the amplifier buffer stage Z34 during Phase 2 by the operation of FET switch Q13 by signal P2, and either +1V or -1V is connected to Z34 during Phase 3 by the operation of FET switches Q6 or Q7, respectively, to reduce the charge on integrating capacitor C49 resulting from conditioned negative or positive inputs.

4.5.1 Phase 1 Operation (Auto-Zeroing).

During Phase 1, the P1 control signal actuates FET switches Q8, Q14, Q16, and Q17.

Closing switch Q17 places integrator Z35 and comparator Z36 in a closed loop while switch Q14 connects zero input to buffer amplifier Z34. During this time switch Q13 is open, and the conditioned input is disconnected from amplifier Z34. The closed loop servoes until all internally generated non-zero signals are balanced at the input to Z35, and the capacitor C48 will be charged with the necessary voltage (amplitude and polarity) to "zero" the loop. (Integrating capacitor C49 will have zero charge.)

At the same time, C39 is charged to the reference voltage in the polarity sense shown, through the charging path including FET switch Q8, FET Q14, and relay KM2B.

4.5.2 Phase 2 Operation (Input Integration).

During Phase 2, the P2 control signal actuates FET switch Q13; if in X.1 range, the gain around amplifier Z34 is multiplied by 10 by closing FET switch Q16 and opening Q15. Otherwise Q15 is closed, for unity gain.

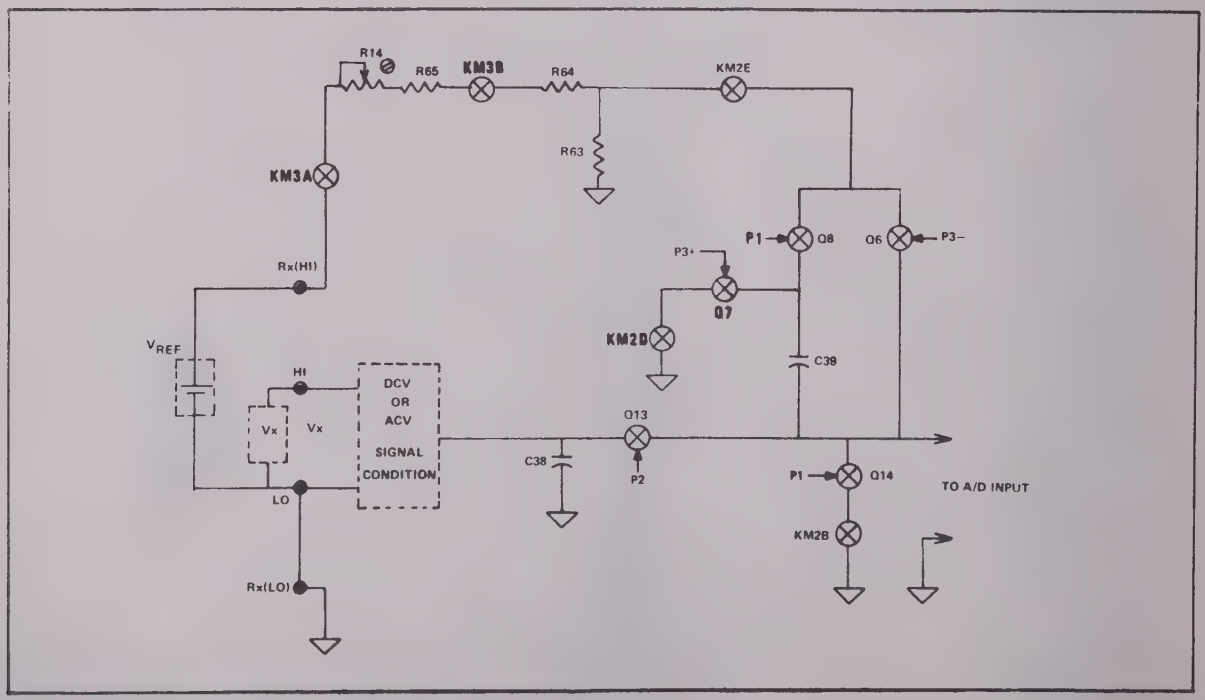

Fig. 4-6. Ratio Measurement Signal Conditioning, simplified schematic

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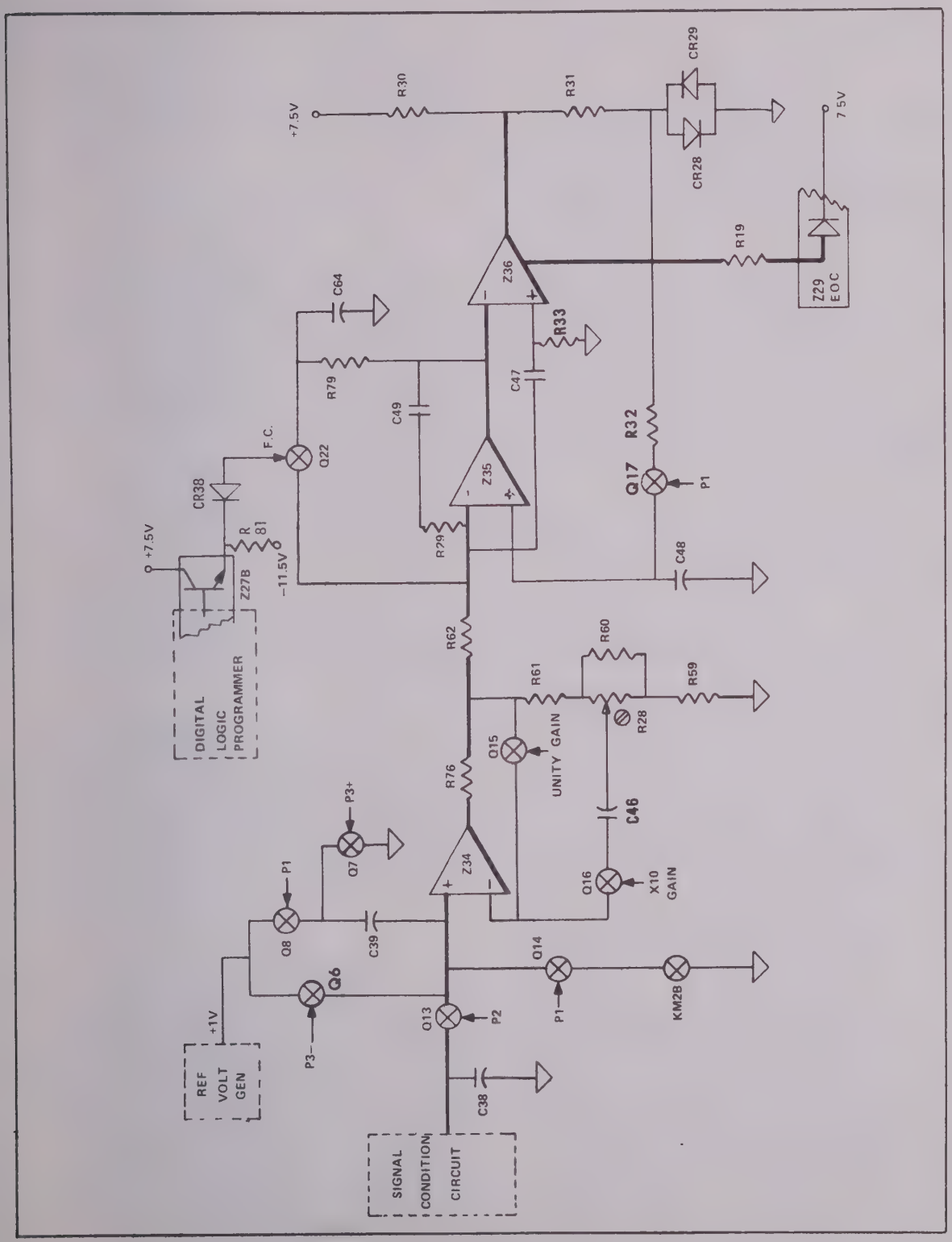

Fig. 4-7. Tri-Phasic A/D Conversion (Analog), simplified schematic

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a. Opening switch Q14 removes the grounding of input to amplifier Z34.

b. Opening switch Q8 leaves capacitor C39 charged to 1 volt with polarity as shown, but it has no effect in this phase.

c. Opening switch Q17 leaves capacitor C48 charged with the "auto-zero" store and provides an offset signal to Z35 that exactly compensates for the non-zero signals within the loop at the end of Phase 1.

The conditioned input, amplified (or not) through Z34, is integrated in Z35 and charges capacitor C49 for the 10,000 count duration of Phase 2. The output of Z35 drives high gain amplifier Z36 to saturation in the same sense as the conditioned input, and the output of Z36 with respect to analog ground is indicative of the polarity of the input. The state of Z36 is translated to suitable drive signal for the opto-isolator and the isolated signal transmitted to the digital logic programmer.

The Phase 2 signal (P2) is a high level for exactly 10,000 counts of the clock. This averaging time base rejects normal mode signals at frequencies of line frequency or integral multiples thereof with extremely high attenuation.

4.5.3 Phase 3 Operation (Reference Integration).

During Phase 3, the digital logic programmer transmits a P3+ control (via opto-isolator) if the conditioned input is positive, or a P3- control if the input is negative.

a. A P3- signal closes FET switch Q6 and connects the +1V level to the input of Z34.

b. A P3+ signal connects the + side of C39 to analog ground, and thus places -1V at the input to Z34.

c. Opening switch Q13 disconnects the conditioned input from the input to amplifier Z34.

d. The stored "auto-zero" compensation on C48 remains to correct for the internal non-zero signals of the integrator-comparator loop.

e. If switch Q16 were closed during P2, it opens, and switch Q15 closes, establishing a unity gain for Z34 during Phase 3. Otherwise Q15 remains closed. (This combination multiplies the gain of buffer amplifier Z34 by 10 while keeping the discharge time the same for full scale inputs. The count is 10X as high, but the decimal point location corrects for this.)

For an in-range input, Phase 3 lasts until the change in state of comparator Z36 output signals the return of integrating capacitor C49 to the initial condition. This change of state changes the level to the opto-isolator, and thence to the digital logic programmer which completes the conversion cycle.

4.5.4 Out-of-Range Control Signals.

If the input signal is out-of-range because it is greater than 100% overrange of the range scale in affect, the change in comparator output state during Phase 3 will not occur within 20,000 counts of the clock. This circumstance is sensed in the digital logic programmer subsystem, and the programmer generates the appropriate out-of-range signal, blanks the display, and provides remote indication of invalid data on the output lines.

When the digital logic programmer circuitry senses the out-of-range condition (no EOC after 20,000 counts in Phase 3), opto-isolator Z27B transmits control signal FC to the analog circuit.

Control signal FC actuates FET switch Q22, closing a discharge path through R79 around integrating capacitor C49. Additional charge that may be needed to reduce the charge on C49 is obtained from capacitor C64.

This action of the fast time constant circuit in out-of-range conditions assures that the integrating capacitor C49 will be at zero charge by the beginning of Phase 1 (auto-zeroing phase), and that the multimeter will be able to operate correctly at designed conversion speeds. Relationships of the voltage levels on C49 when fast time constant discharge is operative are shown in Figure 4-8.

4.6 DIGITAL PROGRAMMING SUBSYSTEM

The Digital Programming Subsystem is instrumented by 3 counters (Z6, Z7, and Z12), Dual J-K Flip Flop (Z8), a scan oscillator, crystal-controlled clock circuit (see complete schematic in back of book), BCD-to-decade decoder (Z25), AND, OR, NAND, EXCLUSIVE OR and NOR gates, and several discrete components (R, C, and Q), as well as the corresponding portions of the opto-isolators that couple the phase control signals to the A/D converter and the EOC/POL signal from the A/D converter to this subsystem.

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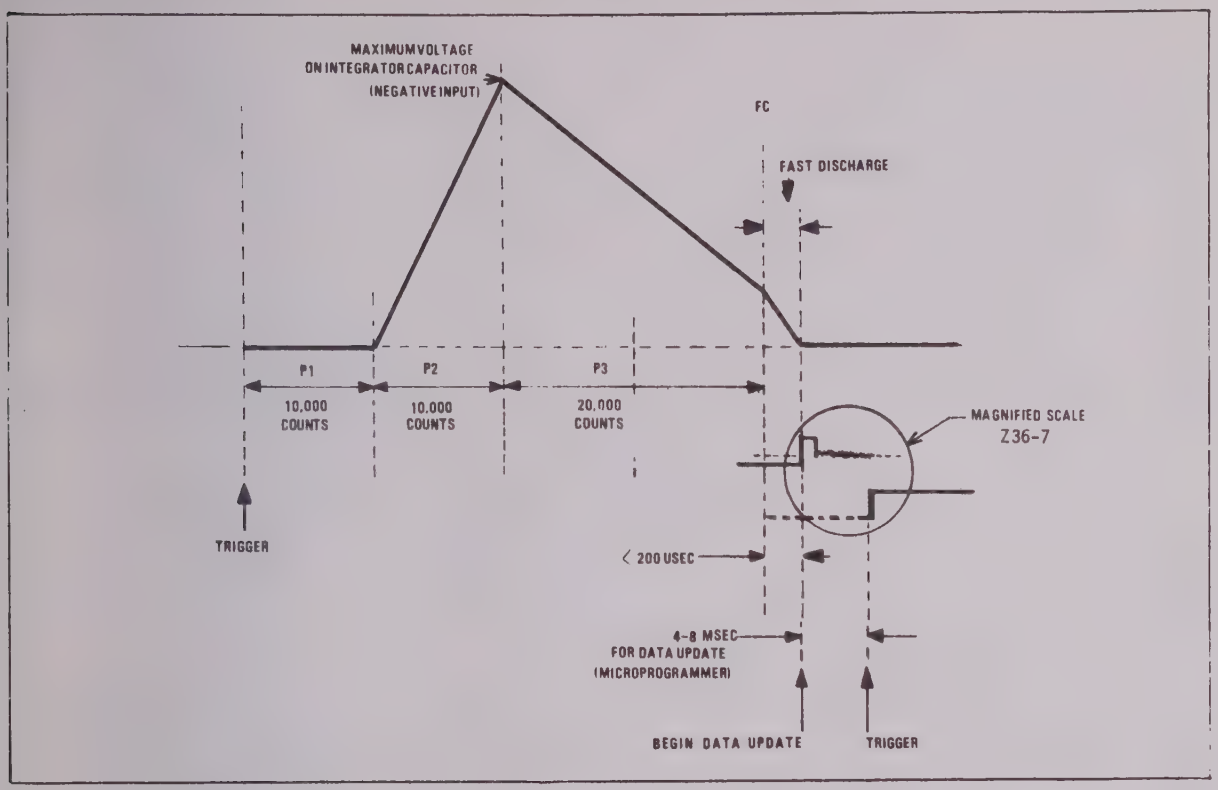


Fig. 4-8. Integrator Capacitor C49 Waveforms - Out-of-Range Conversion Cycle

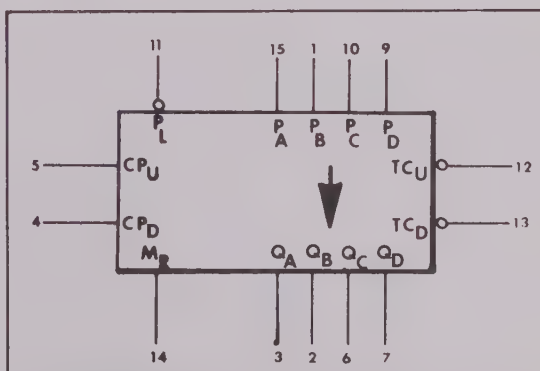
4.6.1 The Programming Counters

The counters in the digital programmer are of two types: pre-settable up-down counters (Z6 and Z7) and 4-decade counter with output register (Z12). As an aid to understand the circuit operation and the description that follows, Figure 4-9 illustrates the truth table logic instrumented in the up-down counter. Figure 4-10 provides a block diagram of the decade counter Z12.

4.6.2 Trigger Generation (Figure 4-11).

The generation of a trigger is enabled by the appearance of a high level at Z6-2, signifying the end of a previous conversion (as described later). The Z6-2 output is one input to AND gate Z28-12. Until Z28-12 is actuated, its output is low, so that the output of gate Z18-11 is high, and no clock pulses are loaded through Z6 to Z12. (Z6-11 needs a low level to LOAD.)

a. Local trigger generation commences with the charging of capacitor C8, started by the High level from Z6-2 at the start of Phase 1.



MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	RESET
L	L	X	X	PRESET
L	H	H	H	NO CHANGE
L	H	CP	H	COUNT UP
L	H	H	CP	COUNT DOWN

Outputs change state after LOW to HIGH of CP_U or CP_D

Fig. 4-9. Up-Down Counter, Block Schematic & Truth Table

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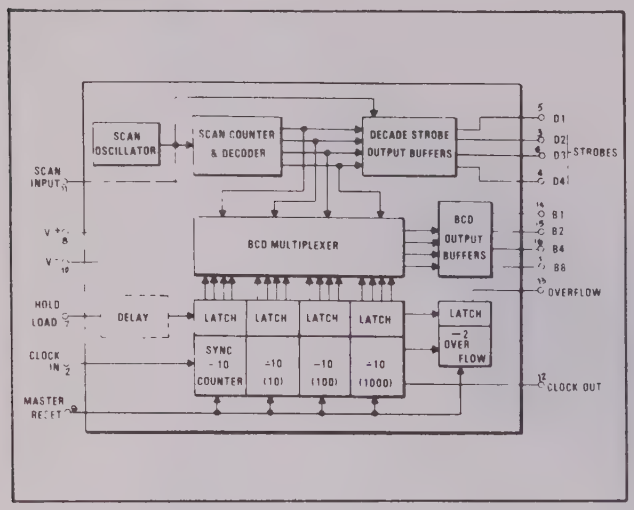

Fig. 4-10 Decade Counter, Block Schematic

(In local control the level of $\overline{\text{HOLD}}$ at pin H follows the level on C8.) At some point in the C8 charge cycle, determined by the time constant of the capacitor and 22K, the charge level exceeds the CMOS level required to change the output state of Z21-4 from low to high, resulting in the third high-level enabling gate Z28-12. This results in the change in state of Z18-11 from high to low and changes Z6 to the LOAD operation.

b. In remote TRIGGER control, C8 is held at the low level by $\overline{\text{HOLD}}$ at pin H. When a trigger is desired, the high level applied at pin F, transmitted through Z21-10 to Z21-4 enables Z28-12. When the next high level from Z6-2 is sensed at Z28-12, Phase 1 counting is initiated as for local trigger operation.

The phase control signal P1 (high) is generated in Z25 as soon as the output level Z6-6 goes high at the end of the previous conversion. Therefore, the analog A/D conversion circuit starts the autozeroing mode immediately after the previous EOC, and remains in that mode for the 10,000 counts that follow the generation of the TRIGGER and enabling of the clock through Z6-7 to Z12-2.

4.6.3 First Carry after Trigger (Figure 4-12).

At the 10,000th count from Z6-7 into Z12-2, a CARRY pulse appears at Z12-12. It is clocked in Z22-8 by the next negative transition of the clock pulse (through EXCLUSIVE OR gate Z18-4) and places a second enabling level at the input to AND gate Z22-6, whose output changes and places Z6 in RESET mode. As a result, all Z6 outputs are set to low level, Z6-6 changes the state of Z28-12 and the output of decoder Z25. At the output of Z25, P1 goes high, while P2 goes low. The P2 low level is transmitted through Z26 (opto-isolator), placing the A/D in Phase 2 operation.

After the carry pulse transition, the reset control is removed from Z6, and the two low inputs to EXCLUSIVE OR gate Z18-11 (from Z6-6 and Z28-12) keep Z6 in load mode, continuing clock pulses to Z12 from Z6-7.

The reset pulse from Z22-6 also maintains Z7 in reset mode through OR gate Z20-11 and after its transition, the low level at Z7-6 connected to Z7-11, places Z7 in load mode. This will permit the transfer through Z7 of the sensed polarity indicated by the A/D comparator output during Phase 2 inputted to Z7-9 from the opto-isolator.

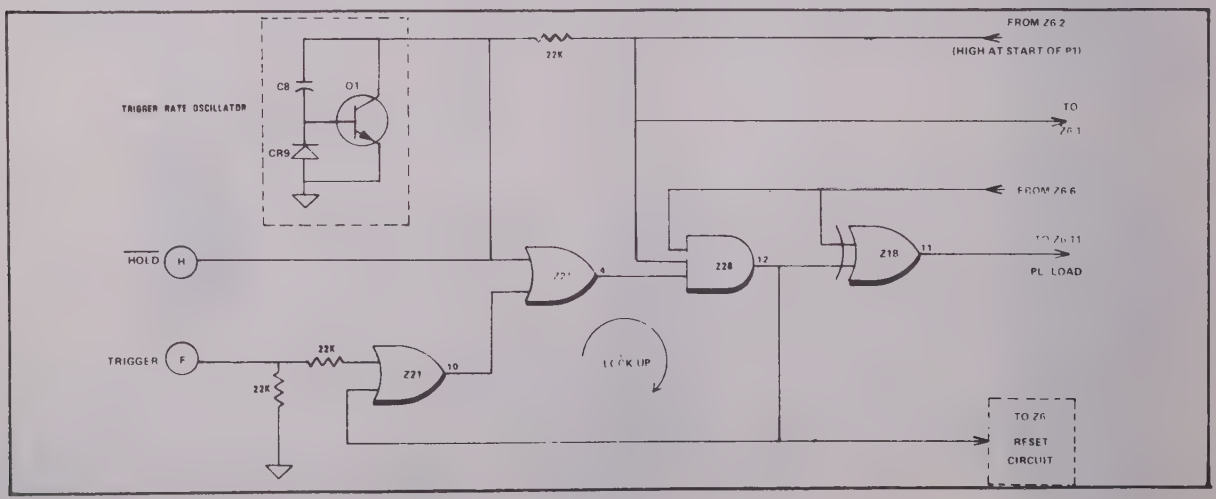

Fig. 4-11. Trigger Circuit, simplified schematic

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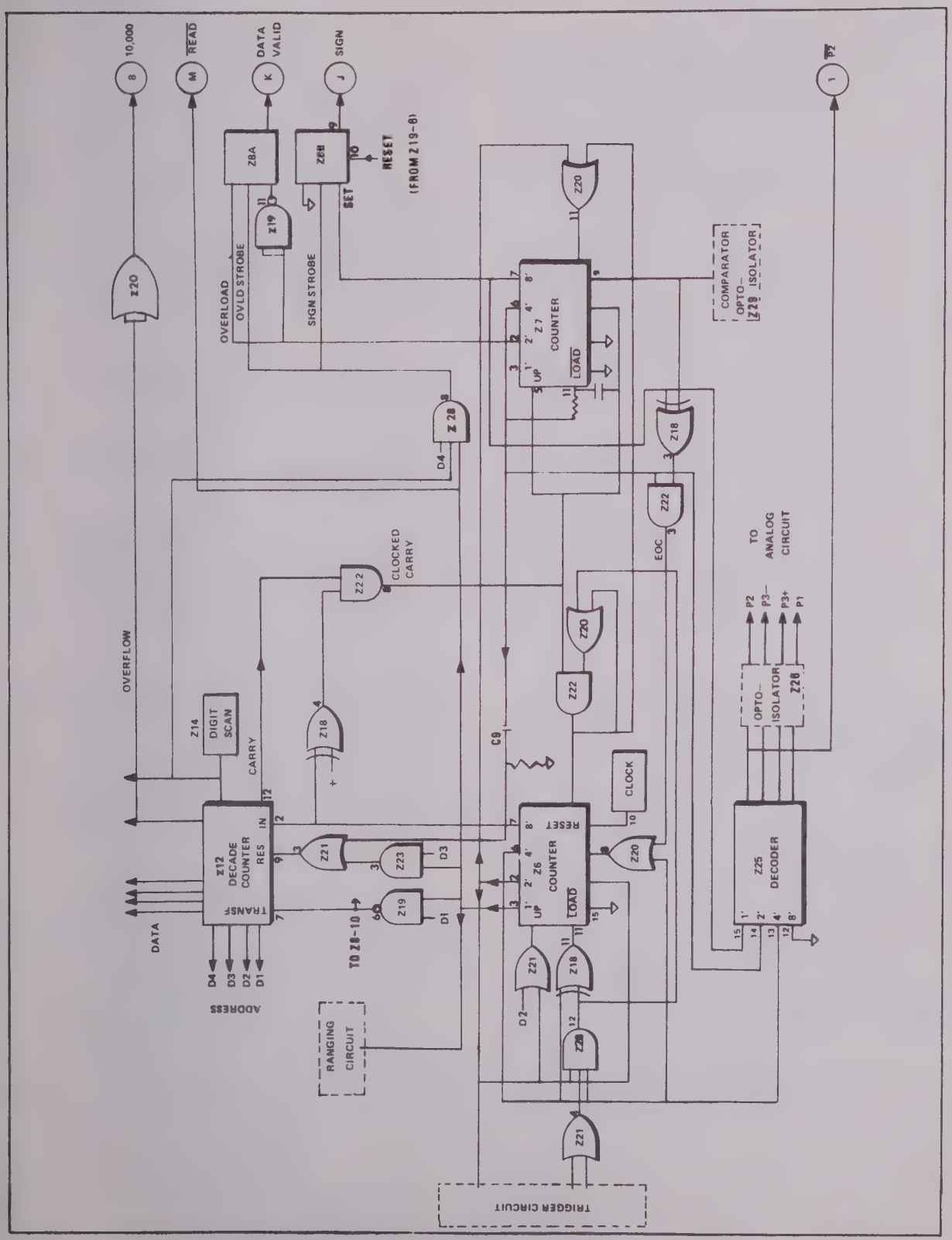

Fig. 4-12. Digital Logic Programming, simplified block diagram

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4.6.4 Second Carry after Trigger.

When counter Z12 reaches 10,000 counts during Phase 2, the carry output is clocked as before, and the high output from Z22-8 is loaded into Z7 so that output Z7-6 goes high.

EXCLUSIVE OR gate Z18-3 will see two inputs of the same level at this time, so that its output keeps gate Z22-3 from changing state when the high of Z7-6 is applied at the input.

The high level from Z7-6 is connected to decoder Z25 (pin 14), and the sensed polarity level is connected to Z25 (pin 15). Decoder Z25 issues a P3- control if the input signal polarity was negative, and a P3+ control if the input signal polarity was positive (2+0, or 2+1).

The low-to-high level transition of Z7-6 is differentiated by C9 and pulses RESET of Z12 at pin Z12-9, through OR gate Z21-3. This action holds the counter at zero (suppressing one count input from Z6-7) assuring the appropriate FET switching actions of the A/D converter have been completed before starting Phase 3.

The high level remains at Z7-6 so that Z7 is in the count mode when the next CARRY occurs, while at the same time enabling Z22-3 for EOC.

4.6.5 Comparator Level Change at End of Reference Integration---In Range.

When the A/D comparator output changes state while in Phase 3, that change is sensed by EXCLUSIVE OR gate Z18-3, which now sees two different levels at its input. The Z18-3 output is applied to AND gate Z22-3, previously enabled by the high level of Z7-6.

The high output of Z22-3, through OR gate Z20-8 loads Z6 so that Z6-6 goes high. The inputs to Z18-11 are now of different levels, so that Z6 goes into the count mode and effectively stops the clock count from Z6 to Z12. Z6-6 also is connected to Z25, transmitting a P1 control level to the analog section.

The following action sequence occurs in one SCAN cycle, controlled by the digit addresses D1, D2, D3, and D4, and which take place in one refresher cycle approx. 4 msec.

At D2, Z6 counts up, placing a high level at Z6-3. This high level is transmitted to output connector on pin M, indicating the measured data values are about to be updated and should not be read.

At D1, Z19-6 changes state, resulting in a low level at Z12-7, placing Z12 in a transfer mode, in which the counter value is transferred to latches, replacing the values of the previous conversion, and thence to the display. It also resets Z8B, setting a "minus" unless changed to "plus" at D4 of the microprogram.

At D4, and synched with the scan osc Z14, Z28-8 changes state and strobes the polarity by transferring the new polarity value through Z8B to pin J at the output connector. It also strobes Z8A, to transfer the input to Z8A to output pin K. Since we have assumed that this EOC occurs at less than 20,000 counts (in-range conversion) the data would be valid and the level at pin K is high.

At D3, AND gate Z23-3 changes state, and its output resets the decade counter Z12.

At D2 (the second count into Z6), the upcount places a low level on Z6-3 and a high level at Z6-2. This is the status at the start of a trigger operation (see para. 4.6.2) and the conversion cycle starts again.

A summary Timing Waveform for the digital logic is shown in Figure 4-16 at the end of this chapter.

4.7 OUT-OF-RANGE

An out-of-range signal is sensed if a third and fourth carry pulse occurs from Z12-12 before the EOC change in comparator output.

On the third carry after trigger, when the input signal is in the 100% overrange specification and therefore "in-range", the clocked output of Z22-8 finds Z7 in a count-up mode (Z7-6 is high, preventing a load mode), and sets Z7-3 to a high level.

On the fourth carry after trigger, the clocked carry input into Z7-5, adds "1" to the counter, sets Z7-3 to a low level, and Z7-2 to a high level. The Z7-2 high level is inverted in Z19-11 and sets Z8A K input to a low level. Z27B is turned on to initiate FC action.

Thereafter, when the change of comparator output state is sensed, the Z8A strobe action described in para. 4.6.5 places a low level output on connector terminal K to indicate that the data output that will appear at transfer action to the output latches is INVALID. The output of Z8A, in addition, is a blanking pulse for the display.

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4.8 RANGE CONTROL & AUTO-RANGING SUBSYSTEM (Figures 4-13, 4-14)

Under manual range control, the sensing of an overload signal and the resulting blanked display, requires a manual change of range to a higher scale, . . . if not already at the highest scale. If data is less than 1/10 of selected range, one may switch to a lower range scale, except if already at lowest range scale, and maintain an in-range reading. Thus, when in auto-ranging, the logic programmer must perform a similar analysis of the circumstances. The logic analysis is instrumented by the combination of NOR gates (Z11-6, Z11-8, Z11-12), AND gate (Z28-6), and NAND gates (Z19-8 and Z19-3), as shown in figure 4-13.

The output of Z19-3 is input to the ranging circuitry (Figure 4-14).

As shown in Figure 4-14 the ranging system (after the logic analysis of Figure 4-13), consists of range counter Z5, decoder Z4, relay and decoder drivers Z2 and Z3, and AND gates Z24-3, Z24-6, and Z24-11.

4.8.1 Decision-Logic Action on Out-of-Range Signal (under range).

The logic requirements for activating a change to a lower range when the conversion is less than 1/10 of full scale are:

a. EOC level is present (conversion is complete)

b. Not at lowest (X.1) range

c. In AUTO ranging mode

d. $\overline{D4}$=0

e. BCD codes are zero

f. 5th decade (MSD)=0

g. Digit scan is high (addresses are not changing)

NOR gate Z11-8 tests:
- Digit Scan = high
- 5th Decade = "0" (M.S.D.="0")
- B1 = "0"

NOR gate Z11-6 tests:
- B2 = "0"
- B4 = "0"
- B8 = "0"

NOR gate Z11-12 tests:
- 4th decade ($\overline{D4}$) is selected
- Auto-ranging = 0 (auto mode)
- X.1 range scale not selected

If any one equality test is not met, then the output of AND gate Z28-6 is low, and when EOC action sets Z6-3 high (see para. 4.6.5), enabling NAND gate Z19-3, its output will be high - - - and no input appears to range counter or to change the input to the VALID DATA flip-flop Z8A. If all conditions are satisfied, then Z19-3 output is low, setting Z8A (indicating no VALID DATA status), and providing a count input to Z5 (Figure 4-14), and calling for a lower range scale.

4.8.2 Range Counter & Decoder Action (Figure 4-14).

As shown in Figure 4-14, the two possible out-of-range conditions for changing range are control signals derived from the Digital Programmer Logic and are inputs to counter Z5. They are:

From Z19-3: A low level indicates the conversion has resulted in a value whose count is less than 1000, and a change to a lower range scale is required.

From Z19-11: A low value indicates the conversion has resulted in a value $\geq$20,000 counts, and a change to the highest range scale is required.

Counter Z5 can respond to these control signals when in auto ranging operation, because the input to Z5-14 will be low, and the reset mode is not effective.

If the decision action requires the highest range scale, Z19-11 is low, Z5 is placed in LOAD mode, transfering the inputs to the outputs and the counter transmits a BCD equivalent of "0" if the measurement function is resistance ($\overline{K\Omega}$ is low), or a "1" if the measurement function is voltage or voltage ratio ($\overline{K\Omega}$ is high). Then decoder Z4 provides a control signal selecting the highest possible range scale (X10K for resistance, X1000 for voltage).

If the decision action requires a lower range scale, Z19-11 is high, Z5 is placed in the COUNT mode, and the counter responds to inputs at Z5-5. Each low-to-high transition occurring at Z5-5 increases the count by one and the corresponding BCD-to-decimal equivalent decoded by Z4 reduces the range scale one step at a time. When the lowest range scale (X.1) is selected, then there is no longer a count input at Z5-5, and the value is at the optimum resolution scale, even though it may be less than 1000 counts.

In summary, when first sensing a value exceeding the selected scale, the auto-ranging circuit selects the highest instrument range scale and steps down in successive conversions. Control signals for the selected scale remain

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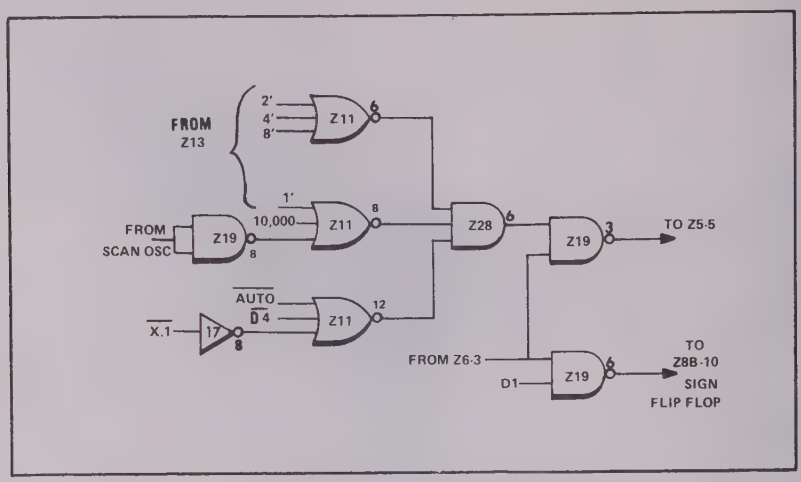

Fig. 4-13. Under-Range sensing simplified block diagram

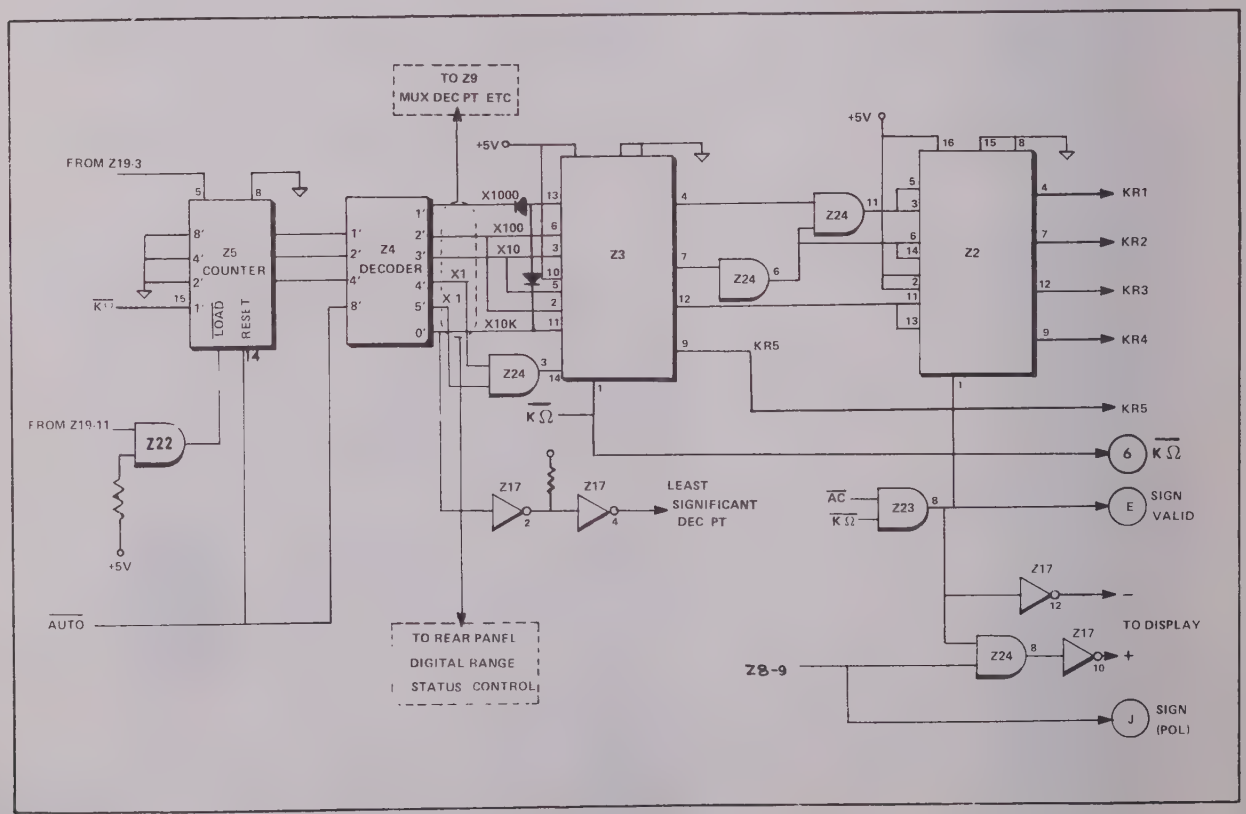

Fig. 4-14. Range Relay, simplified block diagram

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active at Z4 outputs so that succeeding conversions are treated as continuation of the process (whether or not the input has been changed). Thus, if one of the succeeding conversions requires a lower range scale, it will be selected automatically without having to start at the highest scale available.

4.8.3 Range Counter-to-Relay Actuation.

Outputs from the range scale decoder Z4 drive switches Z2 and Z3, whose outputs are logically combined in accordance with the range relay requirements of Table 4-1, and converted to relay-driving signals.

When in auto-ranging, the status of the range-scale selection by Z4 are outputs at the rear connector.

When in manual ranging, front panel switching or remote programming may introduce control signals on these lines and accomplish the range selection. (See Reference Schematic.)

4.9 DISPLAY SUBSYSTEM

4.9.1 Input to Display.

a. The Display Subsystem is continuously updated with the data at the output of Z13, the decimal point from Z9, and the polarity from Z8. The digital data and decimal point are multiplexed under control of the scan oscillator Z14, while the polarity is a steady state signal strobed out of Z8 at the end of each conversion cycle. Annunciators in the display are turned ON by the selection of the measuring mode.

b. When the decade counter Z12 is strobed by the appearance of a transfer signal at pin 7 the counter value is transferred to the output registers in Z12, replacing the values previously stored there. Then, as controlled by the scan oscillator, the contents of each decade are transferred to the Z12 output lines so that the BCD codes for each decade are available at the output terminals 14, 15, 16, and 1 for B1, B2, B4, and B8 respectively. The decade digit for the available BCD data is identified by a high level on the appropriate address line outputs of Z12 for D1, D2, D3, and D4. The value for the fifth digit, D5, is continuously available at Z12-13, and indicates a count of 10,000 when in-range (Figure 4-10).

c. Decimal data for the 4 least significant digits are transferred to drivers in Z13, whence they are transmitted to the Display assembly and to the rear panel connector through output storage latches Z15 and Z16 for remote display and control operations. Outputs of Z13 also drive the logic circuitry for out-of-range control (Figure 4-13).

d. The polarity sign in the display is not active when in either ACV or kilohms, or ACV RATIO measuring modes because AND gate Z23-8 places a low level on the control lines to the Display assembly for these measuring modes. The polarity sign output indication is a single line (terminal J), and the validity of the sign signal is indicated by the level at terminal E, SIGN VALID.

4.9.2 Display Schematic (Drawing 35-1038).

The referenced drawing appears at the back of this manual. The four binary bits for the BCD code are translated into appropriate 7-segment drives by Z1 and are applied in parallel to all 5 decade digits, while the power for each digit is multiplexed in synchronism with the digit value through independent drivers Q1 thru 5.

The selected decimal point is also refreshed at the multiplexed scan rate. Note that the left hand decimal point for each decade is controlled by the selection of the appropriate lower five range measurement scales. The X10k scale requires a right hand decimal point, and this is separately controlled by the range scale selection through Z17-4.

4.10 POWER SUPPLY (Drawing 35-1042)

4.10.1 Sourcing the Model 3400DMM.

a. The Model 3400DMM may be sourced from either 115 or 230 VAC, 60 Hz to 400 Hz power. The power supply generates isolated and shielded analog circuit supply voltages of regulated +7.5 VDC, unregulated +12.5 VDC, and a precision thermally stabilized reference voltage of +6.2 to 6.4 VDC. In addition, the power supply provides the +5 VDC for the digital circuitry through regulator Q2.

b. The input power voltage is filtered, fused (F1), and switched (S3) to the primary of transformer T1 which has been configured by the rear-panel mounted slide switch S4 to accept either 115 or 230 ACV source voltage. Both transformer secondaries are shielded from the primary, and the 19 VRMS secondary (developing the isolated analog circuit power) is shielded from the 8.4 VRMS secondary (for the digital supply).

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4.10.2 Isolated Analog Supply.

The analog supply voltages are developed from the 19-volt transformer secondary in a full-wave rectifier circuit consisting of CR33(KBP-02), followed by dual tracking regulator Z39, which is partially controlled by CR35 and Z38. The full wave rectifier outputs are filtered by capacitors C57 and C58 and supply the ±12.5V supply. Regulator Z39 develops a constant current determined by R66 and from which a negative supply (-7.5V) is determined by the selection of R67. The positive output of Z39 is regulated by servoing a divided portion of its value with reference to the temperature controlled CR35. This provides +7.5V at extremely good regulation, as well as the +6.2 to 6.4 volts for reference in the Phase 3 integration. Internal circuitry divides the stable reference supply from CR 35 to the value of +1V used in the A/D converter during Phase 3.

4.11 LOGIC TIMING

Figure 4-15 illustrates the development of the logic timing waveforms through the digital circuitry.

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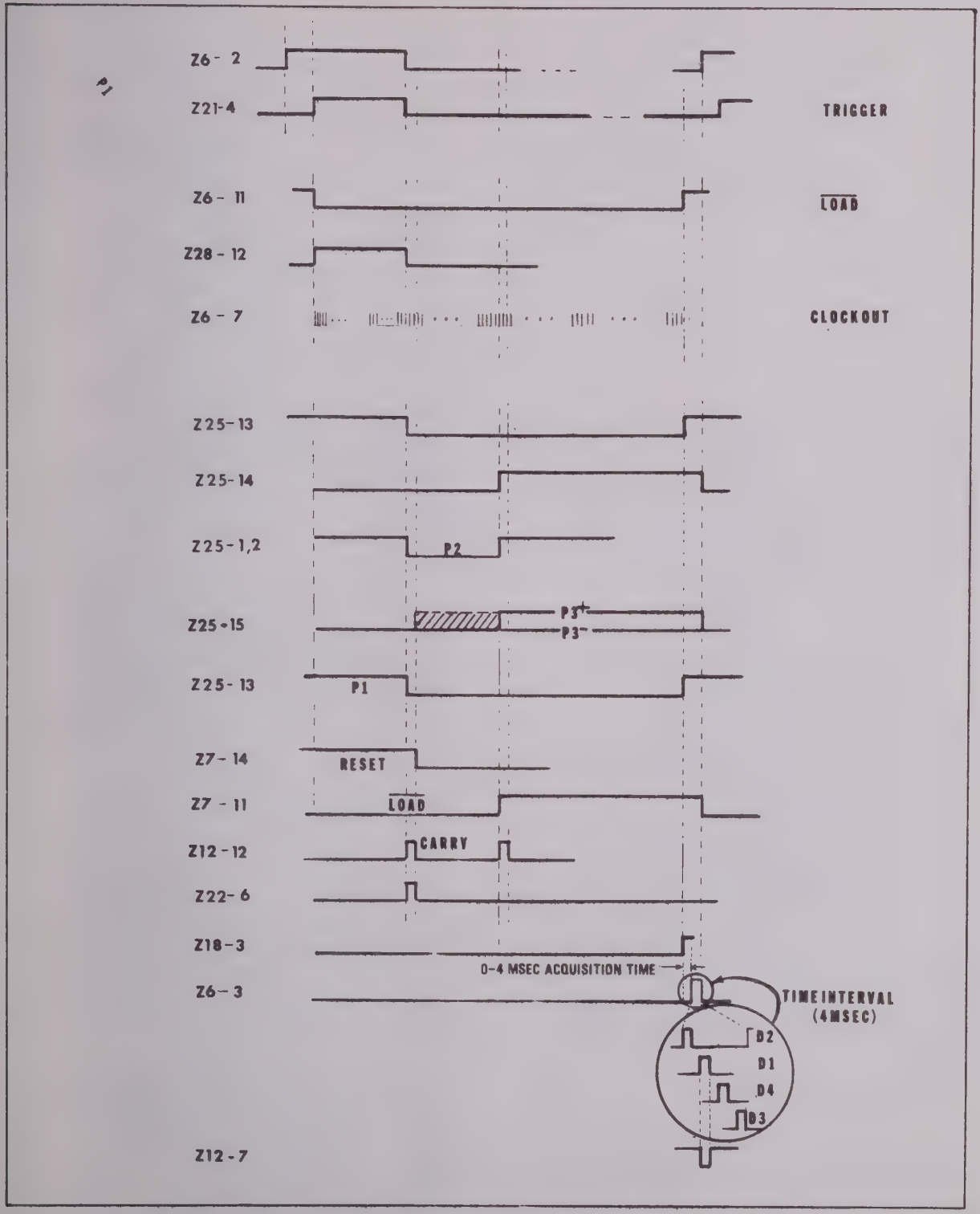

Figure 4-15. Digital Logic timing waveforms.

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5
MAINTENANCE

5.1 GENERAL

a. Model 3400 Digital Multimeter uses solid state components and integrated circuits, and is designed for reliable long-life operation. Except for calibration verification, no operator maintenance should be required, and there should be no normal requirement for opening the DMM case. Should any malfunction require corrective action within the warranty period, arrangements should be made to obtain factory assistance.

CAUTION

Data Precision provides this Maintenance Information primarily for users of Model 3400 Digital Multimeter in need of repair after the expiration of the Warranty period. The information is intended for users who are qualified and competent to effect any needed repairs. The equipment may be returned for repairs at a nominal fee if the user should elect to have the factory make repairs.

b. Should the qualified user attempt to trouble shoot and repair the DMM, he will find that Model 3400 DMM contains a number of features especially designed for simplified unambiguous trouble shooting and fault indication. Among these are:

Full and complete design and parts data in this Instruction Manual;

A positive trouble shooting procedure intended for effective use by competent technical personnel in isolating and correcting all but the most subtle and intricate problem source;

Mechanical parts layout and identification for logical and easy location.

5.2 PARTS GROUPING AND THE TEST STAND-OFF GRID

a. The printed circuit board (Figure 5-1) shows the grouping of major multimeter functions. These correspond, generally, to the schematics in Section 6. When the GUARD is removed, the floating Analog power supply and the analog portion of the A/D Converter and Signal Conditioner are revealed.

b. Verifying signal values throughout the circuit is considerably simplified mechanically by strategically positioned test-points, connected to circuit components for easy access to points where performance may be monitored. Each test point is identified by an E-number on the schematics and screened on the PC-board. Access to every major critical portion of the circuit has been assured.

5.3 TROUBLE SHOOTING STRATEGY

5.3.1 Overview

a. Figure 5-2, which is a fold out at the back of this chapter, illustrates the overall approach to trouble shooting the Model 3400. As illustrated, when a malfunction is perceived, the trouble shooting procedure commences with a thorough checking of possible external causes. Paragraph 5.4 indicates the areas of concern that may be traced to non-meter causes of malfunction indications.

b. Assuming the I/O conditions are satisfactory, the next step in trouble shooting is the analysis of closed-case meter performance. It is possible to verify the proper operation of a number of multimeter subsystems by observing the meter performance in response to some simple stimuli. It may also be possible to identify specific digital logic subsystems as sources of malfunction by interpreting the closed-meter performance. The tests and the subsystems checked or to be checked are described in para 5.5.

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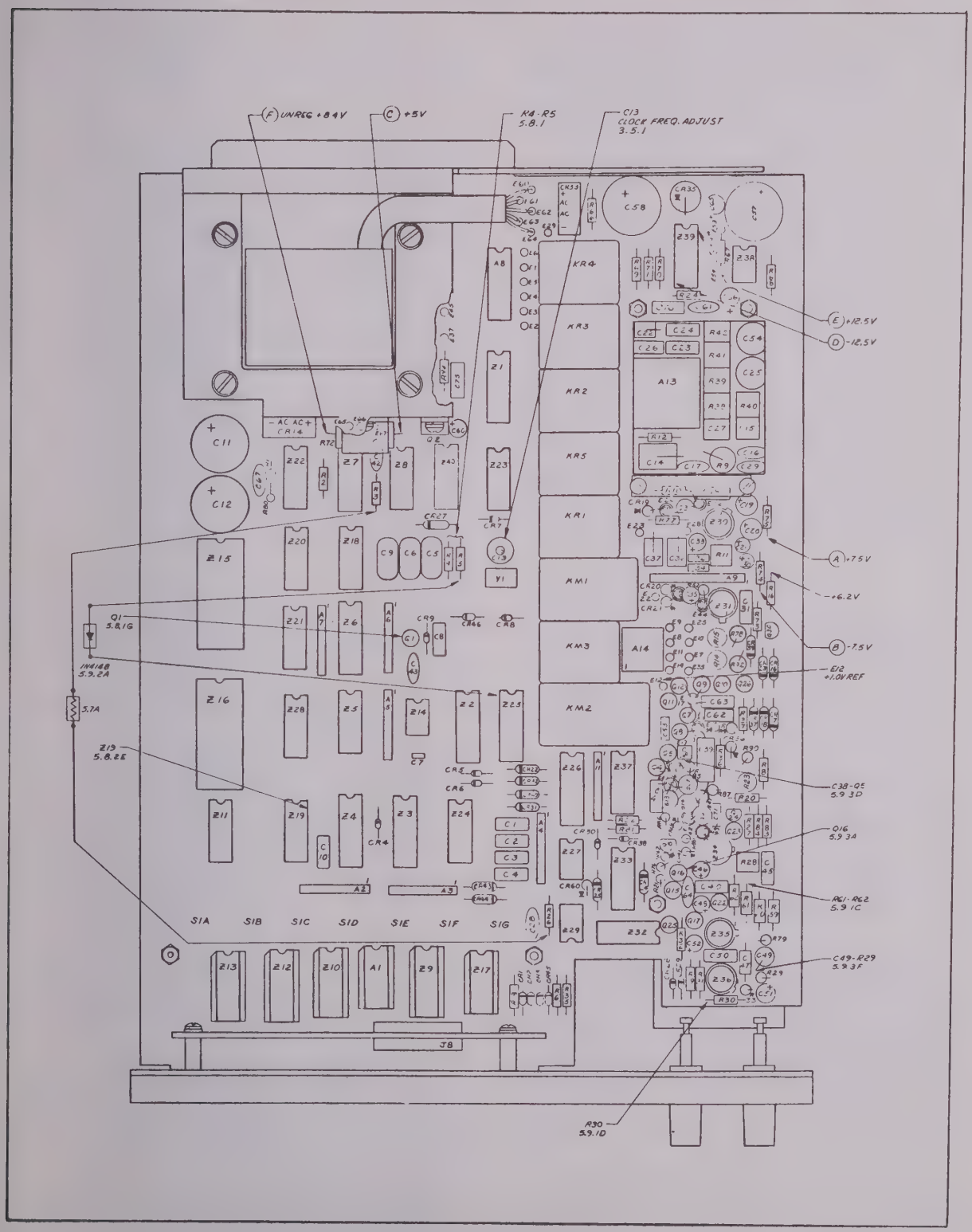

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c. After reasonable assurance that the interfaces with the unknown input are satisfactory, and that we have obtained as much information as possible by observing the closed-case performance, the trouble shooting analysis proceeds with an examination of the open-case instrument. Symptoms of trouble that may become apparent from tactile, olfactory and visual inspections are identified in paragraph 5.6. Paragraph 5.6 also includes the checks one may perform on the power supply, assuming the results of the sensory inspections are satisfactory.

d. It is possible to isolate the source of trouble (if the earlier tests do not clear the malfunction) to either the digital or to the analog circuitry, and these checks are described in paragraph 5.7. The digital subsystem may be divided, for trouble shooting purposes, into the programming logic, display logic, and ranging logic sections. Each such section is checked according to procedures described in paragraph 5.8.

e. As shown in Figure 5-2, signal tracing through the analog-to-digital converter is to be performed after the digital circuitry is checked out (whether or not the digital circuitry needs repair).

f. It will be noted, in Figure 5-2, that the strategy requires a reexamination of the performance after repair and/or replacement (R/R) procedure. When the malfunction is caused by degradation or failure of an analog circuitry component, then a recalibration is necessary. It is also desirable to check the calibration if there is any possibility that calibration-sensitive settings may have been disturbed during the trouble shooting procedure.

5.3.2 Personnel Considerations

The instructions contained in this chapter are intended to assist qualified technicians; they are not expected to be all-inclusive or all-exhaustive to the extent that they will pin-point the cause of malfunction, in every instance, to the malfunctioning component. As stated previously, they are intended to lead the trouble shooter to the cause of malfunction by isolating the apparently proper functioning subsystems. The best preparation for trouble shooting is a thorough understanding of the principles of operation, and technicians are urged to review the material in Chapter 4.

5.4 EXTERNAL/INTERFACE CHECKS

a. With power OFF, examine the multimeter carefully for signs of physical damage such as loose covers, loose binding posts, connectors, frayed or cut power cord, etc. Check to see that the line voltage switch on the rear panel is in the proper position for the power sourcing used (115 or 230 VAC). Check the fuse in the rear panel and verify that it is still intact.

b. Trace the ground circuit to assure that ground loop currents are minimized. Verify that the 3400 DMM rear panel chassis is connected to a good earth ground. Consider the consequences of some finite resistance in the ground leads and the existence of potential differences at respective "ground" terminals.

c. Check the connections for measurement modes as described in Chapter 2. See that shorting links supplied with the multimeter are removed, except between GUARD to Vx Lo when appropriate. Check the "unknown" source circuit.

d. Repair all damaged parts; tighten loose connections; repeat measurement sequence that gave rise to initial evidence of malfunction. If still present, leave power ON and perform the trouble shooting sequence of paragraph 5.5.

5.5 CLOSED-CASE OPERATIONAL CHECKS

5.5.1 Display

a. One may obtain confirming evidence of the proper operation of portions of the display subsystems if the malfunction is not of the "castropnic" kind. That is, when the multimeter displays some value in response to an input, although that value appears to be unrelated to the applied input.

b. Adjust the input over a range of values and observe the 7 segments of each display digit. If at some time each segment is lit at least once, one may conclude that the digits and their drivers are functioning satisfactorily. If the brilliance of all segments are about equal in intensity, then this indicates apparent proper functioning of the multiplexing circuitry.

c. Operate the range select pushbuttons in sequence and observe the corresponding decimal point locations. If satisfactory, then the display decimal points, their drivers, the decimal point multiplexing circuit, and range select switches are functioning.

d. Operate the measuring function pushbutton and observe the corresponding annunciator lights in the display. Their proper operation checks the circuit operation of Z1 in the digital section, as well as the functioning of the display LED's.

e. Select DC measuring function; connect a dc voltage source; observe polarity of display. Reverse input connections and observe

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change in polarity of display. Appearance of both plus (+) and minus (-) signs indicates proper functioning of DS1 in display assembly, as well as polarity-sensing logic in digital section.

f. Failure to observe proper operation of some of the circuitry identified in a through e above (but not in all) is an indication of probable failures in the display or program sections of the digital circuits. As shown in Figure 5-2, these symptoms should serve to "set flags A and B" for the trouble shooter when he reaches paragraph 5.8 in this sequence.

5.5.2 Ranging Circuits.

a. With input configured for 2-wire resistance measurement, select KΩ measuring mode and remove all inputs (open circuit at Vx). The proper response of the multimeter should be a blanked display except for the decimal point. Select a range other than 10k; the decimal point should be displayed in one of the left locations. Select AUTO, and observe the decimal point. Proper operation of the ranging circuits should result in positioning the decimal point to the right of the least significant digit.

b. Improper ranging operation, indicated by incorrect decimal point location or by improper blanking, is a reason for "flag C to be set", and in itself is diagnostic information to be used for the Range Circuit checks of paragraph 5.8.

5.5.3 Front-End Analog Circuit Check

a. With input configured for 2-wire resistance measurement, short terminals by connecting a good conductor between Vx Hi and Lo. Select Range X.1.

b. Operate measuring mode pushbuttons and observe display (if operational). If the value is near-zero for each mode except RATIO (or approximately the same non-zero), then one may conclude that the front-end connections are functioning properly.

5.6 POWER CHECKS

5.6.1 Opening the Case

a. Turn power OFF. Unplug unit from line power. Remove two screws holding top cover to case front and rear, and retain; remove top cover. Check to see that calibration procedure is still cemented to underside of top cover. Remove the three screws fastening the guard over the analog circuitry, and remove guard shield. Inspect the visible assembly. Look for signs of malfunction such as any loose parts (shake the unit), discoloring of the board as a result of heated components, or the odor of burned components, or board. Identify the geographic area of any apparent problem and relate to the corresponding circuit schematic. Set appropriate diagnostic "flags" for later detailed circuit tracing.

b. Replace the line cord plug.

CAUTION

Raw ac power is not normally accessible at the top of the main assembly. However, observe care in handling the assembly for possible appearance of high voltages where transformer malfunctions have accurred, or where the GUARD is driven at a high voltage.

c. Turn power ON. While equipment is warming up, touch the tops of IC's and note excessive temperature on any except the power supply solid state elements. Although warm, the non-power supply units should not be uncomfortably hot when working properly. Locate and correlate the geographic/circuit sections as in b. above, and set flags for subsequent trouble shooting actions.

5.6.2 Regulated Voltage Checks

a. Use DC Voltmeter, ±10.000V range, accuracy at least ±0.05%. Measure voltages with respect to Rx Lo (See Figure 5-1), and check for values below.

Point A (R75 lead): +7.5V + 0.12, -0.16
Point B (R74 lead): -7.5V - 0.12, +0.16

b. To check the digital circuit supply voltages, use DC voltmeter, ±10.000V range, and make measurement with respect to digital ground at the binding post on the rear panel. Note the jumper between E37 and E45 which may be a convenient location for the digital ground connection. The voltage should be checked as follows:

Point C (R72): +5V ± .25V

If the voltage reading is higher than toleranced, replace Q2. If low, check the temperature rise in Q2 by touching its case. It should be hot, but not too hot to touch for a second or so. Short circuiting of any circuit component that causes the reduced voltage may also result in other symptoms of heat: odor, discoloration, etc. Reexamine the board as in 5.6.1 above. Faulty operation of CR14, C11, or C12 may also cause low output.

5.6.3 Unregulated Voltage Checks

To check the unregulated digital and analog supply voltages, use DC Voltmeter, ±10.000V

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range (where 100% overrange is available). Measure voltages with respect to Rx Lo, and check for values as listed below (with nominal line voltage):

Point D (copper run to Z31 pin 7: +12.5V ± 5%
Point E (copper run to Z31 pin 4: -12.5V ± 5%
Point F (with respect to DIG GND) +8.4V ± 5%

5.7 DIGITAL OR ANALOG?

a. Turn power OFF.

b. Install a 10 kilohm jumper between Z7-6 and Z29-7. See Figure 5-1; note that the connection points are picked up at their respective connections to R3 and R26.

c. Turn power ON. The connection mode in b. above should force a zero time interval for phase 3, and thus a zero output value to the display. Deselect all range and mode pushbuttons. If display is +00000, then the malfunction is most likely in the analog circuitry, since the correct display values indicate that the programming logic is operating properly. If the display is not +00000, then the trouble shooting procedure begins with the digital circuit, as indicated in Figure 5-2. Begin the digital circuit trouble shooting with paragraph 5.8 and the analog with paragraph 5.9.

5.8 DIGITAL CIRCUIT TROUBLE SHOOTING

.8.1 Clock & Timing Logic Program*

a. Use oscilloscope with at least 5 MHz bandwidth and examine waveform at Z6-9 with respect to digital ground. The Z6-9 input should be sensed at the junction of R4 and R5 (See Figure 5-1). The frequency of the clock should be 600 kHz* ±0.20 kHz and the scope time base should be adjusted accordingly. Use oscilloscope X10 probe, and adjust scope vertical scale to be able to verify that clock pulse amplitude exceeds 4.5V and that duty cycle is about 50%. Proper display indicates proper operation of Y1 and Z18-10 circuitry.

b. With 10K jumper of 5.7 in place, check the operation of Z6 on the clock input to it by observing the input to Z12-2. Observe a pulse burst of 33 1/3* milliseconds duration corresponding to phases 1 and 2. If not, check the status of load and reset signals on Z6-11 and Z6-14 respectively, and the truth table of Figure 4-9.

c. Check for CARRY output at Z12-12. It is clocked through Z22-8, and thence to counter Z7. Clocking of Z22-8 is controlled by action of Z18-4 while the count or load action on Z7-5 and Z7-10 are determined by the truth table (Figure 4-9) and the signals on Z7-11 and Z7-14 as for Z6.

d. Check for TRANSFER pulse at the input to Z12-7. Its appearance at the frequency of 3 to 5 per second is evidence that the digit scan decoding in Z12 is functioning (providing a D1 input to AND gate Z19-6).

e. TRIGGER check. Check waveform at J9 pin H (HOLD) at rear panel connector. A pulse waveform at frequency of 3 to 5 per second indicates proper operation of internal trigger circuit Q1 (see Figure 5-3).

f. RESET Check. Synchronize the scope with the RESET control pulse from Z7-6 (connection at the R3 terminal is recommended as shown in Figure 5-1). Observe the pulse output at Z12-9 which should appear at start of sweep and be ~4.5V in amplitude. This pulse masks the first count after the second carry. Pulse width should be 1.8 usec to 2.2 usec.

g. TRIGGER, HOLD, and READY (remote)

1. Connect collector of Q1 to DIG GND (Q1 emitter). Use scope to observe absence of clock at gated output Z12-2.

2. Connect J9 pin 7 (READY) to J9 pin F (TRIGGER). Observe narrow positive pulses about 0.4 u sec wide at interval of 39 1/3 msec ±2 msec at Z23-6. This also checks minimum trigger width to which the Model 3400 DMM will respond.

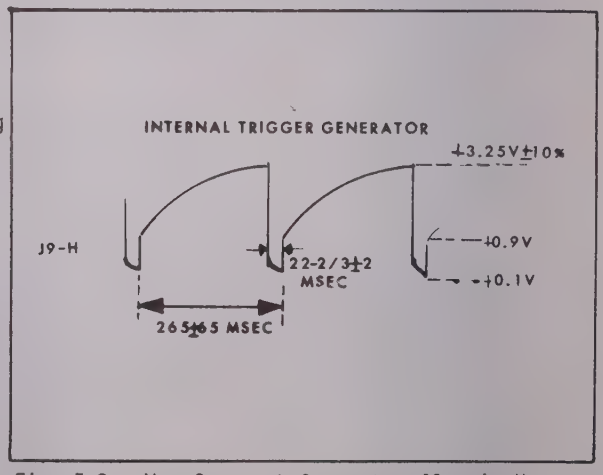

Fig. 5-3. Waveform at Connector J9, pin H.

* The nominal frequencies and cycle times are listed for Model 3400 DMM units intended for use with 60Hz power mains. When the Model 3400 is used with 50Hz mains, the nominal clock frequency is 500kHz and cycle time is 40 msec.

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5.8.2 Display Logic

a. The scan oscillator Z14 operation is checked at its output, Z14-3, by observing the waveform on the oscilloscope. See Figure 5-4 for proper amplitude and frequency of the waveform.

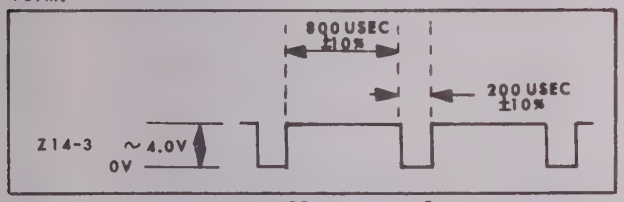

Figure 5-4. Scan Oscillator waveform

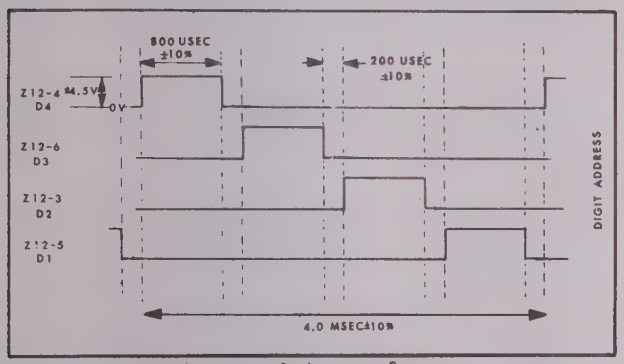

Figure 5-5. Address Code waveforms

b. The operation of Z12 in generating a proper address code can be checked at the output of Z12 by observing the waveforms as shown in Figure 5-5. Note the timing separation between pulse rise and fall events of proper operation.

c. Proper operation of the digit address drive Z10 is checked by examining the waveforms at Z10 which should be the inverted form of Figure 5-5 at Z10-2, Z10-3, Z10-5, and Z10-10, respectively, for D1, D2, D3, and D4 addresses. Output at Z10-1 for the D5 address should be low for 200 u sec ±10% and high for 800 u sec ±10% and should occur at four times the frequency of D1, D2, D3, or D4. Zero level of the output waveform should be ≤0.7V and high level should nearly equal the digital circuit supply circuit whose nominal value has been measured in paragraph 5.6.

d. To check the proper operation of the decimal point control logic for an in-range and underrange input, proceed as follows:

(1) Connect 10K jumper between Z7 pin 6 and Z29 pin 7. (Access to these points are better available at their junctions with R3 and R26, respectively, as shown in Figure 5-1.)

(2) Deselect all range and mode pushbuttons.

(3) Observe display of +00000. No decimal points and all digits of equal intensity.

(4) Select Ranges X.1 through X10K and observe progression of decimal point from left to right. Annunciator should be blanked.

(5) Select AUTO ranging and observe decimal point progress from right to left and value of +.00000 on display.

e. Check logic circuit operation for an overload condition as follows:

(1) Remove R3 terminal of 10K jumper as of 5.8.2 d. Connect it to Z19-12 and -13 (bussed together as shown in Figure 5-1).

(2) Observe display; check for blanked value, decimal point in X1000 position, and positive (+) polarity sign.

(3) Select AC measuring mode. Observe that the polarity sign is blanked.

(4) Select KΩ measuring mode. Observe move of decimal point to x10K (extreme right) position.

Verified performance indicates proper operation of Z11, Z28-6, Z19-3, Z5, and Z4.

Table 5-1

Annunciator and Mode Logic Table

MODE RELAY KM1	KM2	KM3	FRONT PANEL CONTROL	ANNUNCIATOR LIGHT ON	REAR PANEL J9, TERMINAL VOLTAGE LEVEL E(SGN V)	5(MODE SEL.)	2(RATIO)	3(AC)	4(DC)	6(KΩ)
0	0	0	N Mode	None	H	L	H	H	H	H
0	0	0	Ratio	None	H	H	L	H	H	H
0	0	1	Ratio & DC	DC Ratio	H	H	L	H	L	H
1	0	1	Ratio & AC	AC Ratio	L	H	L	L	H	H
0	1	0	Ratio & KΩ	KΩ	L	H	H	H	H	L
0	0	0	DC	DC	H	H	H	H	L	H
1	0	0	AC	AC	L	H	H	L	H	H
0	1	0	KΩ	KΩ	L	H	H	H	H	L

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5.8.3 Ranging Circuit

a. Select KΩMode and deselect range.

b. Check rear panel output terminals J9, C, D, 17, 18, 19, and 20 for all high levels, ≥4.5V. Observe that RANGE SEL at J9 pin 21 is low (permitting remote selection of range.)

c. The ranging relays KR1 through KR 5 and the corresponding levels on the rear terminal should respond to the actions of the front panel controls (See Chapter 4).

5.9 A/D ANALOG CIRCUIT SIGNAL TRACING

5.9.1 A/D Auto-Zero Checks

a. Place voltmeter probe on Z37-13. Connect 10K jumper from Z7-6 to Z29-7. Select DC mode, Range X1. Connect collector of Q1 to DIG GND. A/D locks in Phase 1 operation.

b. Check dc voltage levels as shown below:

Z37-13:	-6.0 to -7.3V	(P2 Drive)
Z37-14:	0 to -0.5V	(P1 Drive)
Z37-2:	-6.0 to -7.3V	(P3- Drive)
Z37-1:	-6.0 to -7.3V	(P3+ Drive)
Z32-10:	0V	Buffer X1 Drive
Z32-11:	0V	Buffer X10 Drive

c. Check voltage at junction of R61 and R62 (Figure 5-1); value should be 0V ± 10mV, and indicates proper functioning of configuration established by Q14 and Z34-Q15

d. Check output of comparator Z36 pin 7 at its junction with R30 (see Figure 5-1). Observe random noise of 1-2V nominal amplitude around ground that indicates proper operation of A/D auto zeroing. Remove jumper around Q1.

5.9.2 A/D Phase 2 Checks

a. Force A/D into Phase 2 by connecting a diode jumper (1N4148) with cathode to Z25-1,2 and anode to R5-C6 junction (See Figure 5-1). Clock is disabled, leaving A/D in Phase 2.

b. Apply input between Vx Hi and Vx Lo over range of ±2V. Check function of buffer amplifier at R61-R62 junction and observe that voltage level follows the input signal.

c. Check dc voltages levels as follows:

Z37-14:	-6.0 to -7.3V	(P1 Drive)
Z37-13:	0 to -0.5V	(P2 Drive)
Z37-2:	-6.0 to -7.3V	(P3- Drive)
Z37-1:	-6.0 to -7.3V	(P3+ Drive)
Z32-10:	0V	(Buffer X1 Drive)
Z32-11:	Negative power rail	(Buffer X10 Drive)

d. Remove diode and 10K jumpers.

5.9.3 A/D Phase 3 (See Figure 5-1 for test points)

a. Select Range X10. Apply -10V at Vx Hi. Synchronize scope on negative transition of gate Q16. Observe Z34 output by connecting scope to R61-R62 junction. Waveform should show switched dc levels from -1V for 16 2/3** msec to +1V for 16 2/3** msec. Display should be -10.000 ± .025.

b. Reverse polarity of input voltage signal. Scope should show switched DC level for +1V for 16 2/3** msec to -1V for 16 2/3** msec. Display should be +10.000 ± .025.

c. Set coarse input to nominal zero volts. Select Range X1. Adjust vernier control of input voltage standard so that display shows all codes between ± 0.0005.

d. Set voltage standard to -10V (range X1) so that overload conditions should cause Q5-C38 (Fig. 5-junction to limit between -3V and -4V. Display should indicate overload blanking of all digits, lighted decimal point and negative polarity sign.

e. Set voltage standard to +10V; observe Q5-C38 junction voltage limits between +3V and +4V, and changed polarity sign on display.

f. Observe output of Integrator Z35 at R29-C49 junction (Fig 4-2) while repeating steps d. and e. that apply overload inputs. Observe the "fast charge" action of Z35 that reduces the output to zero. Remove scope probes.

5.10 RECALIBRATION

Remove all jumpers
Replace Guard Shield. Replace Top Cover
Repeat calibration of Chapter 3.

** 20 msec for 50Hz power mains

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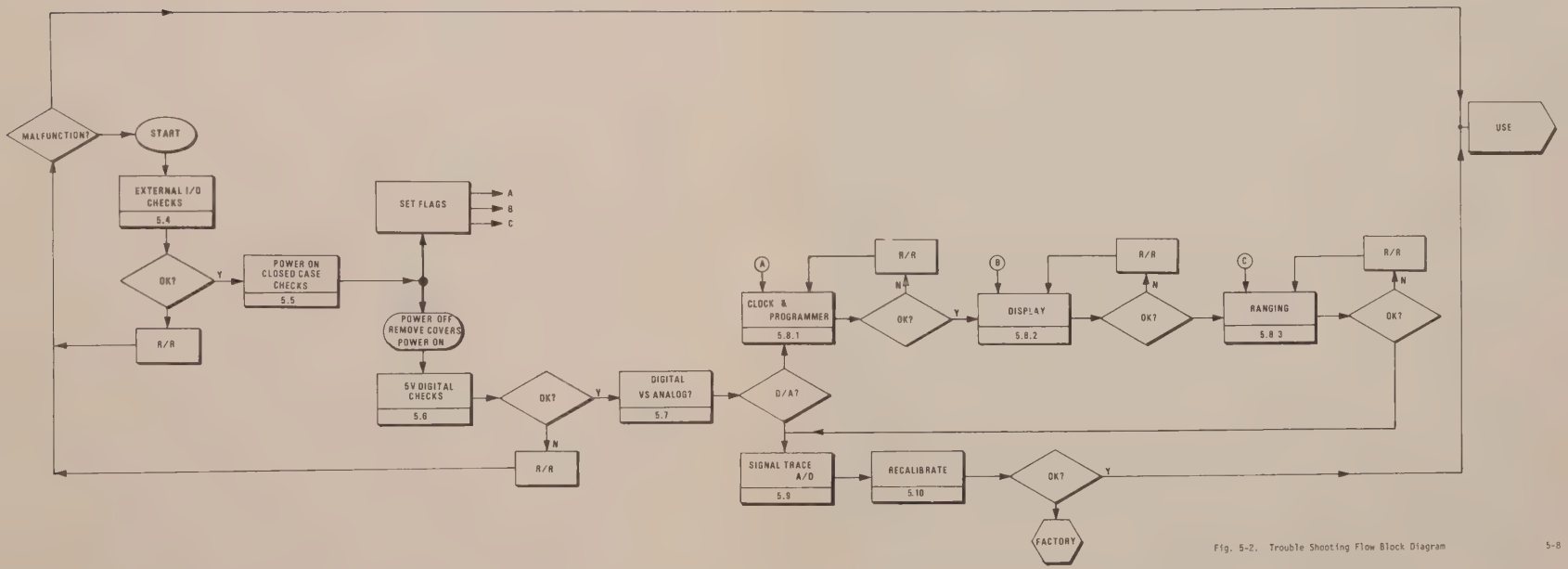

Fig. 5-2. Trouble Shooting Flow Block Diagram

Chapter 6

PARTS LISTS (REPLACEABLE ELECTRONIC PARTS)

6.1 MAIN BOARD ASSEMBLY

6.2 DISPLAY ASSEMBLY

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6.1 MAIN PC BOARD ASSEMBLY

REF SYMBOL	DESCRIPTION	PART NUMBER
A1	RES NET 2.2K 2% DIP	22-701002
A14	RES NET	22-38-1043
A2,3,7,11	RES NET 2.2K 2% SIP	22-730001
A4	RES NET 220 2% SIP	22-730000
A5	RES NET 15K 2% SIP	22-731000
A6	RES NET 22K 2% SIP	22-731001
A8	RES NET 2.2K 2% DIP	22-711000
A9	RES NET	22-38-1036
C13	CAP TRIM .10-60 PF TOP ADJ	23-810008
C1-4,10,61	CAP CERM .1UF 12V 20%	23-118206
C11,12,57,58	CAP AL ELL 2500UF 16V	23-620005
C19,20	CAP TANT 68UF 20% 15V	23-442004
C21,46,48,51,52,59,60,65,66	CAP ELEC TANT 15UF 10V 20%	23-441003
C43,75	CAP CERM .001UF 20% 1KV	23-118202
C28,64	CAP CERM 0.2UF 12V 20%	23-118003
C30,35	CAP ELEC TANT 6.8UF 25V 20%	23-441005
C32,34	CAP CERM 2.7PF 50V .25PF	23-110002
C33	CAP ELEC TANT 1UF 35V 20%	23-441001
C36,37	CAP PC, 1UF,50V 10%	23-510001
C38	CAP PSTY .018UF 50V 10%	23-550105
C39	CAP PC 0.47UF 50V 10%	23-510018
C40,50	CAP DIP MICA 51PF 500V 5%,DM15	23-311006
C41	CAP DIP MICA 10PF 500V 5%,DM10	23-310002
C42	CAP CERM 180PF 10%, 1KV	23-111073
C47	CAP MYLAR .0033UF 80V 10%	23-210311
C49	CAP POLYPRO 0.1UF 200V 10%	23-580001
C5,18,31,71	CAP DIP MICA 150PF 500V 5%,DM15	23-311015
C6,45	CAP DIP MICA 27PF 500V 5%,DM15	23-311041
C53,62,63	CAP CERM .01UF,150V Z5V 60%-40%	23-111006
C7	CAP CERM .022UF 10% 50V	23-140100
C8	CAP CERM .068UF 50V 10%	23-140061
C67	CAP,DISC,390 PF,1KV	23-111074
C76	CAP,82PF,500V,5%	23-111008
CR1-9 ,19,28-30,34,38,41,60	DIODE SILICON 1N4148	24-110001
CR22,24-27,31,32,36,40,43,44	DIODE GERM 1N270	24-140270
CR14,33	DIODE 100V BRI REC FW-100	24-100019
CR16,17,23,39	DIODE RECT 1N4004	24-104004
CR18,37,42	DIODE ZENER 1N746	24-120062
CR20,21	DIODE SCHOTTKY 5082-2800	24-110004
CR35	DIODE RED (SEL A38-1045)	24-130004
CR45,46	DIODE,ZENER,1N702	24-120002
J8	CONN PC AP929636-02	25-690069
KM1	RELAY 4 FORM C AZ 429-V12-202	38-1037-2
KM2	RELAY 6 FORM C AZ 439-202-200	38-1037-3
KR1-5,KM3	RELAY 2 FORM C AZ 428-V09-200	38-1037-1
OVEN	OVEN KLIXON 3ST1-2	25-250000
Q1	TRANS SI NPN 2N3565	24-233565
Q4,Q5	TRANS FET N CHANNEL ORANGE	24-48-1014-10
Q7,Q8	TRANS FET N CHANNEL YEL/WHT	24-48-1014-09
Q23	TRANS FET P CHANNEL RED OR GRAY	24-38-1046-01 or 02
Q24,28	TRANS SI NPN MPS 2369	24-232369
Q27	TRANS FET P CHANNEL RED	24-38-1046-01
Q3,9-12,15-17,22,25	TRANS FET N CHANNEL YEL	24-48-1014-05
Q30	TRANS SI NPN MPS 6515	24-236515
Q6,13,14,26	TRANS FET N CHANNEL BRN/WHT	24-48-1014-04
R1,2,22,27,36,77,83,88	RES 2.2K 1/4W 5% CARBON	22-022229
R10	RES 15K 1/4W 5% CARBON	22-021539
R11	RES TRIM 1K 20% ZA1022	22-666102
R25,52,81,87	RES 100K 1/4W 5% CARBON	22-021049
R14,15	RES TRIM 500 20% ZA 5012	22-666501
R20,26,82	RES 1MEG 1/4 5% CARBON	22-021059
R21	RES 43K 1/4W 5% CARBON	22-024339

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6.1 MAIN ASSY(CONT.)

R19	RES 300Ω1/4W 5% CARBON	22-023019
R67	RES RN55C 18.7K 1% MET FILM	22-341872
	RESISTOR SET	22-38-1044
R59	RES PRECISION 1.87K	22-38-1044-2
R61	RES PRECISION 16.9K	22-38-1044-1
R23	RES TRIM 25K 20% ZA 2532	22-666253
R24	RES 20K 1/4W 5% CARBON	22-022039
R28	RES TRIM 2.5K 20% ZA2522	22-666252
R29	RES 16 1/4 5% CARBON	22-021609
R3,79	RES 200 1/4W 5% CARBON	22-022019
R30,68	RES 750 1/4W 5% CARBON	22-027519
R31,32	RES 33K 1/4W 5% CARBON	22-023339
R33	RES 3.3K 1/4W 5% CARBON	22-023329
R35	RES 1.6K 1/4W 5% CARBON	22-021629
R37,74-76,86	RES 100 1/4W 5% CC-(ONLY)	22-021019-C
R4	RES 7.5K 1/4 5% CARBON	22-027529
R5	RES 2MEG 1/4W 5% CARBON	22-022059
R6,73	RES 4.7K 1/4W 5% CC-(ONLY)	22-024729
R60	RES RN55D 17.8 1% MET FILM	22-3317R8
R62	RES RN55D 66.5K 1% MET FILM	22-336652
R66	RES RN55C 71.5K 1% MET FILM	22-347152
R69	RES RN55C 931 1% MET FILM	22-349310
R70	RES RN55C 4.99K 1% MET FILM	22-344991
R71	RES RN55C 158 1% MET FILM	22-341580
R78,92	RES 100K 1W 5% CC	22-041049
R8	POS 7.5K 40% @ 25C 500V RATING	22-991000
R80,R84	RES 240 1/4W 5% CARBON	22-022419
R85,R18	RES 22 1/4W 5% CARBON	22-022209
R94	RES 51 1/4W 5% CARBON	22-025109
R95	RES 27K 1/4W 5% CC	22-022739
S1	SWITCH PB 7 STA SCHADOW F S	38-1039
Y1	RESONATOR CERAMIC VERNITRON	38-1038
Z1,4,10,25	IC BCD TO DEC DECO/DRI	24-A74145
Z11	IC TRI 3 INPUT NOR GATE	24-E0LS27
Z19	IC QUAD 2 INPUT "NAND" GATE	24-C74L00
Z12	IC 4 DECADE COUNTER W/LATCH	24-G06010
Z13	IC QUAD 2 INPUT MUX LPTTL	24-C93L22
Z14	IC TIMER 555	24-400555
Z15,16	IC DUAL 4 BIT LATCH LPTTL	24-C93L08
Z17	IC HEX INV BUF/DRI	24-A07406
Z18	IC QUAD "EXCLU OR" GATE	24-G34030
Z2,3	IC QUAD 2 INPUT MUX TTL 9322	24-A09322
Z20	IC QUAD 2 INPUT"OR" GATE	24-E0LS32
Z21	IC QUAD 2 INPUT "OR" GATE CMOS	24-G34071
Z22,Z23,Z24	IC QUAD 2 INPUT "AND" GATE	24-E0LS08
Z26	IC QUAD OPTO ISOLATOR ILQ-74	24-NILQ74
Z27	IC DUAL OPTO ISOLATOR ILD-74	24-NILD74
Z28	IC TRIPLE 3 INPUT "AND" GATE	24-E0LS11
Z29	IC SINGLE OPTO ISO 5082-4350	24-N04350
Z30,31	IC OP AMP 301AH LIN TO-5	24-420301-01
Z32	IC QUAD 2 INPUT "NAND" GATE	24-L04011
Z33	IC HEX INV DTL 9937	24-469937
Z34	IC OP AMP LF356H LIN TO-5	24-420356
Z35	IC OP AMP CA3130T LIN TO-5	24-423130
Z36	IC COMP 311H LIN TO-5 GRN DOT(SEL A32-3015)	24-420311-01
Z37	IC QUAD COMPARATOR 2901	24-402901
Z38	IC OP AMP LM741C RED DOT(SEL B42-1006)	24-400741
Z39	IC LIN VOLT REG DUAL RC4194D	24-404194
Z5-7	IC BINARY HEX UPDOWN CTR	24-C93L66
Z8	IC DUAL J-K FLIP-FLOP DTL 9094	24-469094
Z9	IC 5 BIT COMP LPTTL 93L24	24-C93L24
Z40	IC HEX INV BUF/DRI,7407	24-A07407

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6.2

DISPLAY PC BOARD ASSEMBLY

A1	RES NET 68 1/8W 2%	22-711001
A2	RES NET220 1/8W 2%	22-711002
A3	RES NET100 1/8W 2%	22-711003
DS1	DISPLAY LED	25-227752
DS2-DS5	DISPLAY LED	25-227750
DS6	DISPLAY LED	25-227778
I1-I4	LAMP LED	25-224695
Q1-Q5	TRANSISTOR,2N5819	24-245819
Z1	INT CKT	24-A07447

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Chapter 7

REFERENCE SCHEMATICS

Analog Schematic:	Dwg. No. 35-1042-Sheet 1
Digital Schematic:	Dwg. No. 35-1042-Sheet 2
Power Supply Schematic:	Dwg. No. 35-1042-Sheet 3
Display Assy. Schematic:	Dwg. No. 35-1038

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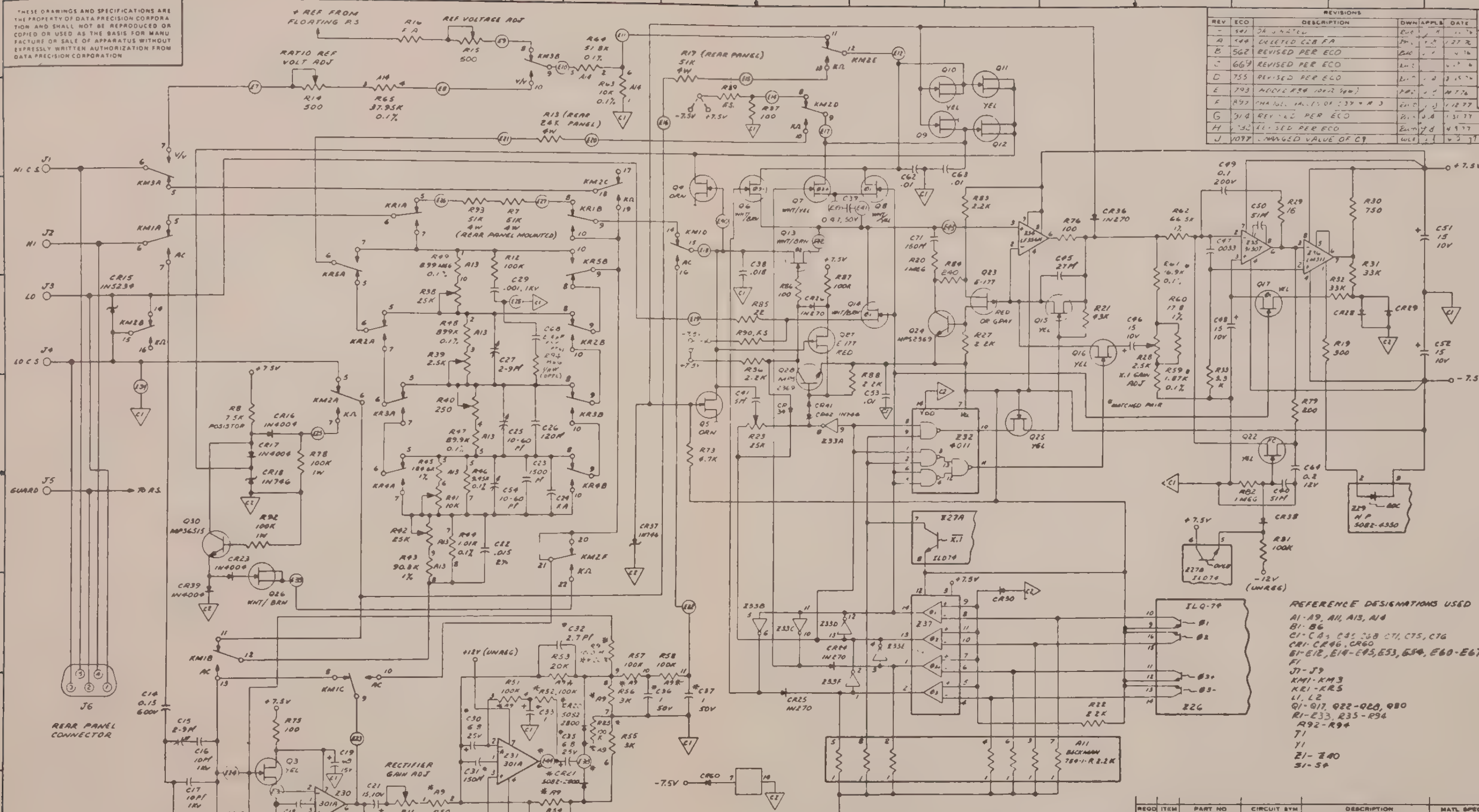
REVISIONS

REV	ECO	DESCRIPTION	DWN	APPLD	DATE
–	541	[illegible]			
A	544	DELETED C28 FA			
B	562	REVISED PER ECO			
C	669	REVISED PER ECO			
D	755	REVISED PER ECO			
E	793	MODIFIE R34 (100Ω ¼w)			
F	897	CHANGED VALUES OF C34 + R 3			
G	914	REVISED PER ECO			
H	932	REVISED PER ECO			
J	1097	CHANGED VALUE OF C9			



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE ¼W, C.C. ±10%, VALUES EXPRESSED IN OHMS
2. ALL CAPACITOR VALUES EXPRESSED IN MICROFARADS
3. ALL DIODES ARE IN4148
4. ALL RELAYS SHOWN IN DE-ENERGIZED POSITION

REFERENCE DESIGNATIONS USED

A1-A9, A11, A13, A14
B1-B6
C1-C43, C45-C68, C71, C75, C76
CR1-CR46, CR60
E1-E12, E14-E45, E53, E54, E60-E67
F1
J1-J9
KM1-KM3
KR1-KR5
L1, L2
Q1-Q17, Q22-Q28, Q30
R1-R33, R35-R94
R92-R94
T1
Y1
Z1-Z40
S1-S4

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

NEXT ASSY	USED ON
AL35-1070	3400A
[illegible]	340

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES

MATERIAL

FINISH

APPLICABLE SPECIFICATIONS

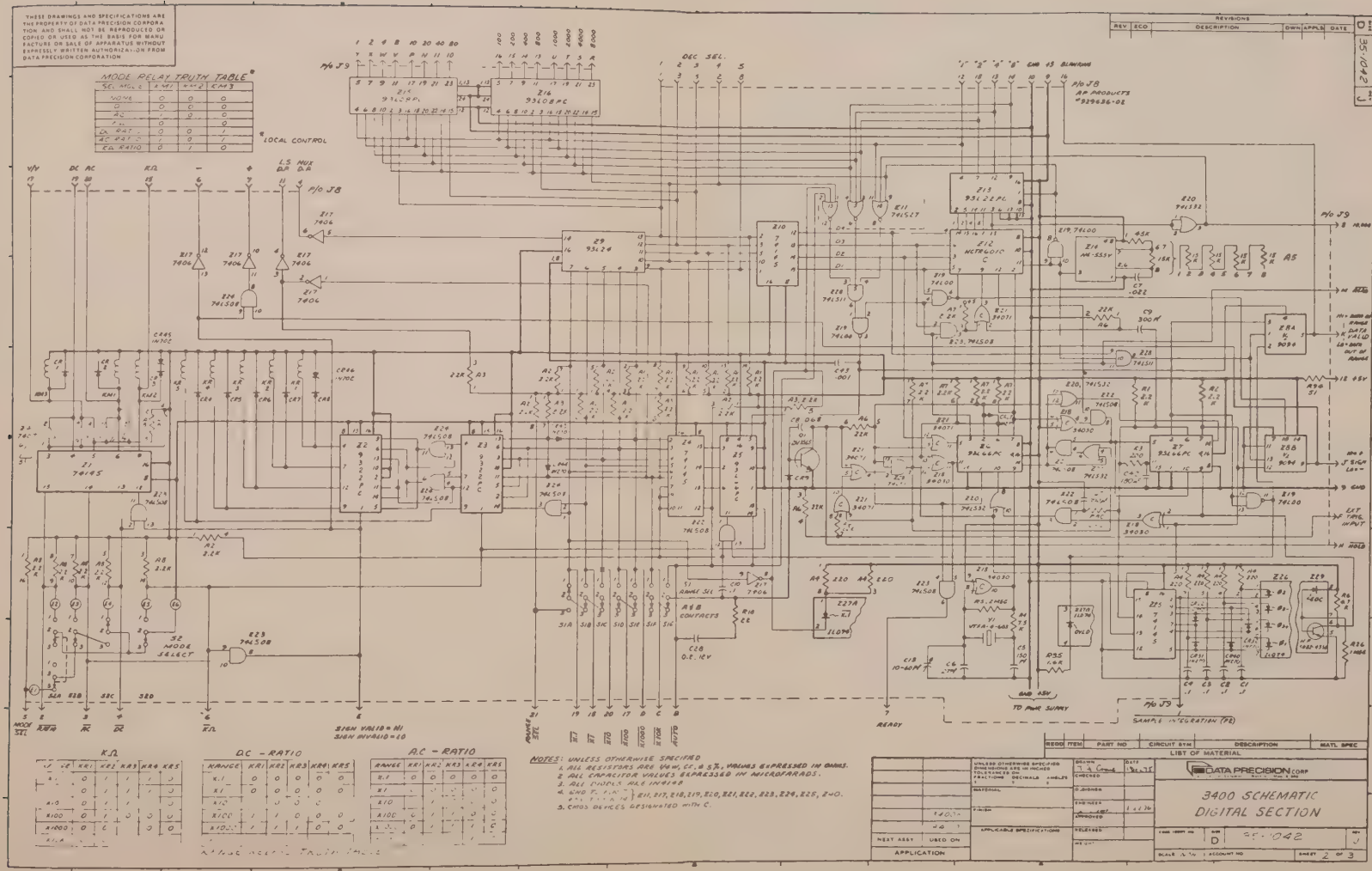
DRAWN / CHECKED / DESIGNER / ENGINEER / APPROVED / RELEASED / WEIGHT

DATA PRECISION CORP

3400 SCHEMATIC
ANALOG SECTION

SIZE D — DWG NO 35 1042 — REV J

SCALE — ACCOUNT NO — SHEET 1 OF 3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REVISIONS
REV ECO DESCRIPTION DWN APPD DATE
D 35-1042 J
MODE RELAY TRUTH TABLE*
SEL MODE K#1 K#2 CR#3
NONE 0 0 0
0 0 0 0
AC 0 0 0
1 0 0 1
CAL RAT 0 0 1
AC RAT 0 0 1
CAL RATIO 0 1 0
*LOCAL CONTROL
DEC SEL.
P/O J9
P/O J8
AM PRODUCTS #9296836-02
LS MUX DA
P/O J8
NOTES:
1. UNLESS OTHERWISE SPECIFIED
a. ALL RESISTORS ARE 1/4 W, CF, @ 5%, VALUES EXPRESSED IN OHMS.
2. ALL CAPACITOR VALUES EXPRESSED IN MICROFARADS.
3. ALL DIODES 1N4148
4. AND F. F.'S Z11, Z17, Z18, Z19, Z20, Z21, Z22, Z23, Z24, Z25, Z40.
5. CMOS DEVICES DESIGNATED WITH C.
MODE SEL
SIGN VALID = N1
SIGN INVALID = L0
RANGE SEL
READY
SAMPLE INTEGRATION (P2)
TO PWR SUPPLY
K Ω
D.C - RATIO
A.C - RATIO
RANGE RELAY TRUTH TABLE
REQD ITEM PART NO CIRCUIT SYM DESCRIPTION MATL SPEC
LIST OF MATERIAL
DATA PRECISION CORP
3400 SCHEMATIC
DIGITAL SECTION
D 35-1042 J
SHEET 2 OF 3
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
APPLICABLE SPECIFICATIONS
DRAWN
CHECKED
APPROVED
RELEASED
NEXT ASSY USED ON
APPLICATION

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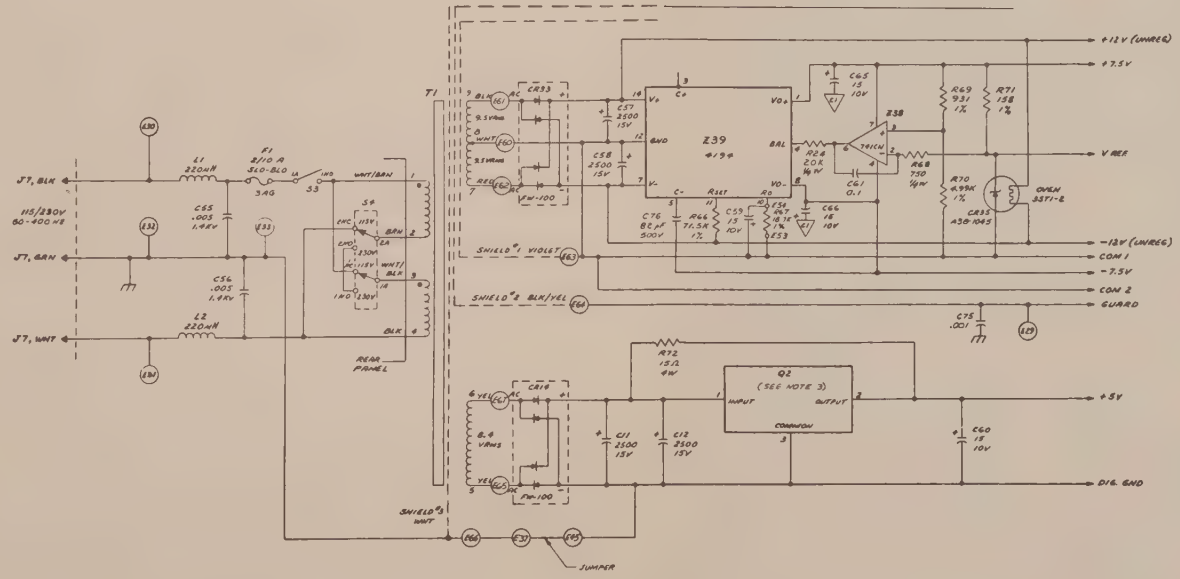
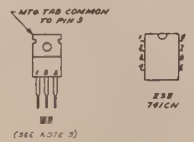
REVISIONS					
REV	ECO	DESCRIPT.	DWN	APPD	DATE

D 35-1042 J





NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL 1% RESISTORS ARE TYPE RN55C, FILM, VALUES EXPRESSED IN OHMS.
2. ALL CAPACITOR VALUES EXPRESSED IN MICROFARADS.
3. Q2 MAY BE EITHER LM340T-5 OR 7805UC.

REQD	ITEM	PART NO	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DESIGN	DATE 4/21/77	DATA PRECISION CORP
	CHECKED		3400 SCHEMATIC POWER SUPPLY
MATERIAL	DRAWN		
FINISH	ENGINEER		
3400R	APPROVED		
APPLICABLE SPECIFICATIONS	RELEASED		DWG IDENT NO D SIZE D REV J
NEXT ASSY USED ON	WEIGHT		SCALE NONE ACCOUNT NO SHEET 3 OF 3
APPLICATION			

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REVISIONS					
REV	ECO	DESCRIPTION	DWN	APPR'D	DATE
—	372	ADD 1 PF TO C1	WC	[illegible]	7-31-75

SEC 01-SE

A2 220Δ

A3 100Δ

A1 68Δ

Q1 2N5819 Q2 2N5819 Q3 2N5819 Q4 2N5819 Q5 2N5819

DS1 H.P. 5082-7752

DS2 DS3 DS4 DS5 H.P. 5082-7750

DS6 H.P. 5082-7778

7447

I1 A.C.

I2 D.C.

I3 KΩ

I4 V/v

MINUS (−) PLUS (+) MUX DP DEC 5 DEC 4 DEC 3 DEC 2 DEC 1

L.S.D. DP DIG GND 1 BIT 2 BIT 4 BIT 8 BIT BLANKS KΩ AC DC V/v +5v

REQD	ITEM	PART NO.	CIRCUIT SYM	DESCRIPTION	MATL SPEC

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWN [illegible]	DATE 7-31-75	DATA PRECISION CORP.
MATERIAL	CHECKED		SCHEMATIC 3400 DISPLAY BOARD
	DESIGNER		
FINISH	ENGINEER		
	APPROVED		
PL30-1061 3400	APPLICABLE SPECIFICATIONS	RELEASED	DWG NO. 35-1038 REV —
NEXT ASSY USED ON		WEIGHT	SCALE ~ ACCOUNT NO. SHEET 1 OF 1
APPLICATION			

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